EE Summer Camp – 2006
Computer Architecture – Tentative Projects

(**Maximum** of **3 projects** from the proposed topics based on interest)
[**Total 5-6 students**]

1. FPGA implementation of a 8-bit processor based on 8051 microcontroller

2. FPGA implementation of a 32-bit RISC pipelined processor with pipeline and bypass.

3. FPGA implementation of an 8-bit RISC processor for calculator.

4. FPGA implementation of a pipelined processor for Image processing/ Digital Signal Processing applications.

5. FPGA implementation of a pipelined processor for data compression (Information theory).

Each of the above projects will broadly consist of these phases:

- Reading about various architectural components of the specific processor.
- Broadly defining the modules of the design and deciding the datapath width, register file size, specific instruction set, etc.
- Writing the Verilog Code for all the modules, integrating them and simulating the processor behavior on ModelSim.
- Porting the Verilog Code to an FPGA (Field Programmable Gate Array) Board to do hardware gate level verification of your design.
- Running simple applications on your FPGA implemented processor.

Note: Your own ideas are also welcome.

Mail us if you need details/clarifications on any of the topics.

Thank you,
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