Computer Architecture Quiz with solutions

Max total time: 10 mins

Abhinav Agarwal

Veeramani V.

1. Trivia 4 mins.

a) Name a CISC processor (1 point)

Ans: Any one of: Intel – 8086, 286, 386, 486, Pentium 1, 2, 3, 4; AMD – Athlon; Zilog – Z80, Z280, etc.

Note: Some RISC processor families are: ARM, MIPS, IBM's PowerPC.

b) What does a compiler do? (2 points)

Ans: It converts programs or source codes written in High Level Languages (C, Java) into Assembly Language code.

c) What does `add r1,r2,r3` mean? (1 point)

Ans: It means add the values stored in registers r2 and r3, and put the sum in r1.

d) CPI of a pipelined processor is around ___(1 point)

Ans: 1.

Note: As the number of independent instructions increase, the CPI tends towards the ideal value of 1, but is always greater than it.

2. Encoding scheme

- In a certain RISC processor's instruction set, there are 63 instructions, and 64 registers in the register file. What will be the minimum length (in bits) of encoded instructions and why? The instruction set also contains arithmetic instructions like add. Explain your answer in brief.

  (5 points)

  Note: Chocolate for the answer we expect. ☺

  Maximum time: **6 mins**

Answer to part 2

- As discussed in class, RISC instructions have simple and fixed encoding schemes which have the same instruction length for all instructions in the set.
- The instruction set comprises of 63 different instructions, this implies a minimum of $\lceil \log_2 63 \rceil$ = 6 bits
- Number of registers in register file = 64

  So, the $\log_2 64$ = 6 bits each are required to specify every operand.
- For, the register-register scheme discussed, there are 3 register addresses for instructions like *add r1, r2, r3* , giving us a total of 24 bits as the min. instruction length.

  6 bits (instruction opcode) + 6 bits (Reg1) + 6 bits (Reg2) + 6 bits (Reg3).

- *Note 1:* Instructions like *mov r1, 24H* also have the same length as the above, in RISC set, because all instructions have to have the same length. The place where we were specifying other register addresses is now occupied by the immediate value 24 H.
- *Note 2:* RISC architectures need not have a Register-register scheme. In an alternate form, called the Accumulator scheme, instructions are of type: *Add B* . This means that add the value contained in reg B to the fixed accumulator reg. Due to only 1 register operand in these instructions, the minimum length for this scheme is 12 bits.

  6 bits (instruction opcode) + 6 bits (Register operand).