

Clock Gating

1. A power saving techniques used in synchronous circuits (i.e. circuits that require a clock for transitions). Extensively used in Intel Pentium 4.
2. Identify portions of the circuit that are currently inactive, retaining their earlier state
3. Use additional logic to disable clock to such inactive state holding flip flops.
4. This helps in reducing two major components of power dissipation:
 - a. Power consumed by flip-flops on each clock edge, even if their inputs are static.
 - b. Power used by clock distribution and buffer network, that distributes the clock throughout the chip, even to areas that currently do not need it.
5. Example: Reference www.aiec.com/Publications/snug2000.pdf

Consider a Traditional 3 Bit Counter:

Verilog Code:

```
module counter (CLK, RESET, INC, COUNT);
input CLK,RESET,INC;
output [2:0] COUNT;
reg [2:0] COUNT;

always @(posedge CLK or negedge RESET)
if (~RESET)
COUNT <= #1 3'b0;
else if (INC)
COUNT <= #1 COUNT + 1;
endmodule
```

The traditional Implementation is seen in Figure 1. The clock is routed directly to each of the flip-flops in the design, which means that they will be clocked continuously, with the old data recirculated into the flip-flops through the multiplexers on the flop inputs, when the *INC* input is low.

In Figure 2, the same circuit is implemented with clock gating. The circuit is similar to the traditional implementation except that a clock gating element has been inserted into the clock network, which causes the flip-flops to be clocked only when the *INC* input is high. In this case a simple 2-input AND gate can be used as the “Clock Gating Circuit”. When the *INC* input is low, the flip-flops are not clocked and therefore retain the old data just as in the original implementation. This allows the three multiplexers in front of the flip-flops to be removed, which can result in significant area savings when wide banks of registers are being implemented.

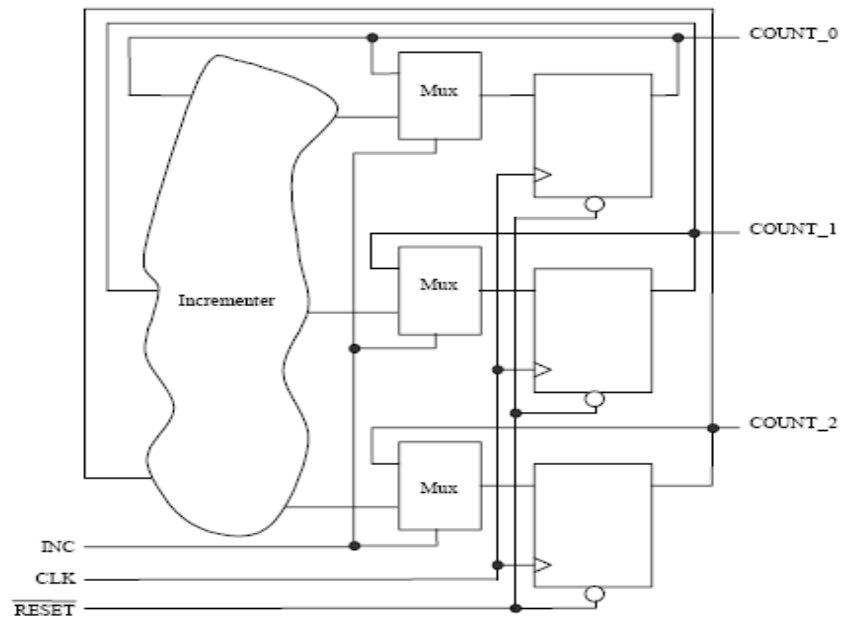


Figure 1 – Three Bit Counter Traditional Implementation

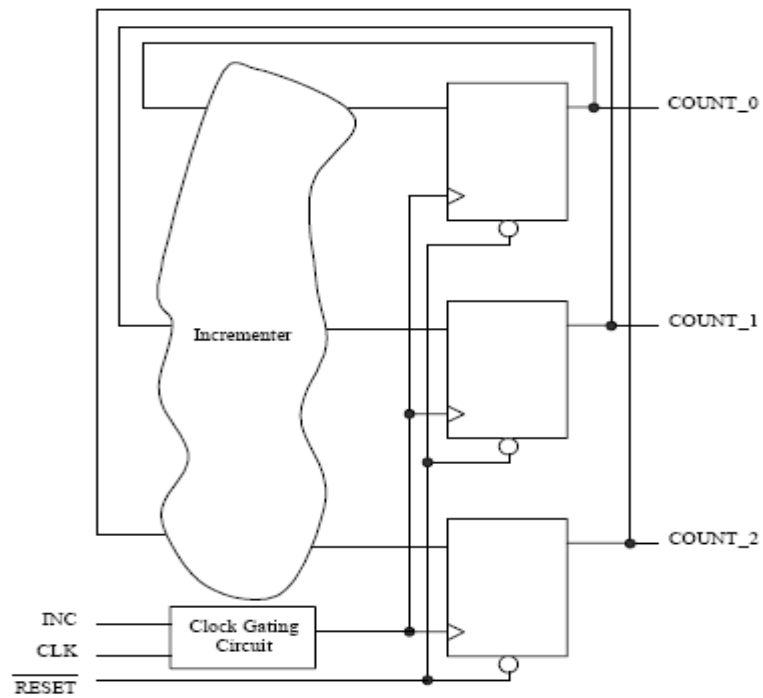


Figure 2 – Three Bit Counter with Clock Gating