M.TECH.THESIS ABSTRACT 1992

Microelectronics, VLSI & Display Technology

Signal processing, Communication & Networks

RF Engineering & photonics

Power & Control

Title : *The Effect Of Ionospheric Scintillation On Image Reconstruction By Synthetic Aperture Radio Telescope*

Author(s) : *Mahajan Rajeev*
Roll No : *9010435*
Supervisor(s) : *Mathur Naresh C*

Abstract

The radio images reconstructed by using Synthetic Aperture Radio Telescopes are distorted due to the effect of ionospheric irregularities. The effects are especially pronounced at lower frequencies. The effects have been studied for the Giant Metre Wave Ra dio Telescope (GMRT) being built at Pune, India. GMRT being a metre wave radio telescope is very susceptible to these image distortions due to the effect of the ionospheric irregularities. A new approach to integrate the work of both the astronomers and th e propagation community has been tried using the mutual coherence function (MCF). Simulations to study the effects of different parameters like frequency, declination, sun spot number etc. have been carried out. The ionospheric irregularities have been mod eled by the WBMOD program for calculation of scintillation indices developed by Fremouw. The effects can be clearly seen in the color coded photographs attached

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Title : Modular Microprocessor Test System

Author(s) : Srinivasan R
Roll No : 9010432
Supervisor(s) : Biswas R N

Abstract

With the aim of designing a suitable test equipment for studding any microprocessor in asimulated environment from a commonly available computer a Modular MicroprocessorTest System has been designed with a PC-AT as the host .It has the capability of handling32-bit microprocessor and has been designed keeping the requirements of CISCprocessor in mind. From the PC-AT, the user can control signals as well as programmeexecution on the target processor and study its response through this system. The TestSystem consists of three modules- PC –Host Interface , General Interface and Target-Specific Interface. The PC-Host Interface module buffers the PC-AT bus from the targetinterface and is produced into an expansion slot on the PC-AT system unit . The GeneralInterface contains all the common block s required to connect the target processor to thePC-AT, while Target-specific Interface contains the processor-related circuitry. Target-specific Interface contains the processor-related circuitry. Target-specific Inter face islinked to the General Interface through a common target bus and up to16 Target-specificInterfaces catering to as many as 16 different processor can be connected to it. The testsystem has been tested with an 8085a development system and satisfied the requirementsfor which it has been designed .This test system is expected to fill a gap in the facilitiesrequired for the design of microprocessor-based systems, namely that of accuratesimulation of a variety of processor and their environment for study and pre-designevaluation.

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Title : *Signal Analysis Using Wavelet Transform*

Author(s) : *Adhikary Ranen*
Roll No : *9010431*
Supervisor(s) : *Gupta Sumana*

Abstract

The thesis is about signal analysis using wavelet transform. Wavelet theory, which has gained a lot of momentum has been investigated. Various orthogonal basis function which make up the wavelets have been analyzed. The corresponding wavelets have be en found out. The filters based on the wavelets/orthogonal basis functions have been designed. A computer program has been developed to do the decomposition and reconstruction of signals based on an iterative algorithm. The signals which have been taken up for analysis are composite exponentials and sinusoidal. The same signals with closely spaced bursts and noise have also been taken up for investigation. A signals have also been decomposed and reconstructed by using another scheme called laplacian pyramid scheme. A separation of exponentials, an age old problem has also been taken up for investigation in this context. The purpose of his investigation is to see whether by during wavelet decomposition and reconstruction, the exponentials which constitut e the original signal, surface or not

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Title : ***A Two Segment Traffic Generator For Testing Ethernet Systems***

Author(s) : ***Kaul T N***
Roll No : ***9010450***
Supervisor(s) : ***Srivathsan K R***

Abstract

A two way traffic generator for loading two Ethernet segment with packets genera t e d under programmable control is designed. O n board intelligence of PCLINK2 Interfaces is made use of, where onboard CPU and LAN coprocessor does the work of transmitting the packets once the packet. (Contents of this packet are programmable upto to network layer header) is downloaded in the shared memory of the interfaces. W hich reduces the data movement over the host bus. LTG so designed is used to test the performance of LAN components, such as R e peater, Bridges and Router, to their saturation limits laid down in IEEE 802.3 Ethernet standards

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Title : *Study Of Line Codes For Fibre Optic Communication*

Author(s) : *Kumar Sujeet*
Roll No : *9010448*
Supervisor(s) : *Chatterjee P K*

Abstract

Line coding is used to improve the transmission reliability over a line (channel). It is the conversion of the input digit sequence to a format which facilitates detection in the presence of usual transmission impairments like base - line wander, inter - symbo l interference, loss of sync etc. line codes provide error monitoring too. In this thesis, line codes used for fibre optic transmission systems have been reviewed. Properties of various line codes, in particular, mBnB block code, mBlC code DmB1M codes and PFmB (m+1) B codes have been discussed in detail. Possibilities of using multilevel codes in a fibre optic link and difficulties obtained have also been discussed. Sensitivities of different front - end optical receiver configuration have also been studied.

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Title	***:***	***Application Of Minimum Shift Keying In Coherent Subcarrier Multiplexing***
Author(s)	***:***	***Shrivastava Pankaj***
Roll No	***:***	***9010428***
Supervisor(s)	***:***	***Sircar Pradip& Chatterjee P K***

Abstract

A multichannel coherent MSK system using subcarrier - multiplexing technique is proposed here. A total of 20 MSK channel at 100 Mbit/second each can be transmitted on one optical carrier using microwave subcarriers in a multioctave configuration. Corsstalk d ue to adjacent channels is negligible with a channel spacing of twice the data rate (200 MHz). A complete description of system performance, including carrier to noise ratio, intermodulation distortion and receiver sensitivity, is given. A similar descript ion is given for multichannel coherent FSK system. The performance results for the MSM system are compared with those obtained for FSK system and the MSK system is shown to have better results

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Title : Design And Implementation Of A Repeater For Ethernet

Author(s) : Narayan A D
Roll No : 9010407
Supervisor(s) : Srivathsan K R

Abstract

A local area network consists of a variety of sub system such as the physical media, host computer interfaces for the LAN, a medium access control mechanism and others. Whenever a LAN such as Ethernet needs to be extended beyond the limits of a physical me dium such as a coaxial cable, due to signal attenuation and distortion the job is done by sub systems such as Repeaters, Bridges or Routers. The repeater is a physical layer device which amplifies and retimes the signal from one side of the network to ano ther within the acceptable delay. In this work, the design and successful implmenation of a Repeater conforming to IEEE 802.3 Ethernet standards is described. The actual implementation details are described after a presentation of an presentation of an ove rview of the Ethernet standard. The hardware has been fabricated in wirewrap form using fast TTI MSI ICs and FIFOs. The performance measurements of the Repeater were carried out on a LAN testbed. The results show that the Repeater has almost no error and c onforms to the standards.

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Title : *Study Of Gibbs Distributed Images*

Author(s) : *Ramesh Chaveli*
Roll No : *9010412*
Supervisor(s) : *Rao P R K*

Abstract

A Gibbs distributed image is one in which the probability distribution of pixel intensities is a Gibbs distribution. The distribution function is characterised by a set of parameters. In this work, an image generation method known as the spin-flip algorithm has bBen used to generate Gibbs distributed images with varying sets of parameters and the effect on the texture of the image of changing various parameters has been studied. Also, an attempt has been made to come up with a parameters estimation method based on histogramming. The method has b&en tested on various simulated images. Further, an image compression method has been proposed that operates by modelling images as Gibbs distributions. A compression ratio of two has been obtained for various simulated images. A texture classifi cation method has been suggested that depends upon minimising the Euclidian norm from the parameter set of the image to the parameter set of each class. Satisfactory results have been obtained

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Title : *Efficent Integration Of Multirate Synchronous And Asynchronous Traffic Services Over Token Ring Type Networks*

Author(s) : *Kazmi Naim Hasan*
Roll No : *9010427*
Supervisor(s) : *Bose Sanjay Kumar*

Abstract

A MAC protocol capable of providing integrated synchronous and asynchronous trafficservice over Token Ring Type Network has been proposed. A simulator, OMNILNA,capable of simulating a network carrying both synchronous and asynchronous traffic wasalso developed. This simulator also has the capability of simulating a system of inter-connected LANs carrying asynchronous traffic only. The simulator can be used to study a system of up to networks; each network can havea maximum of 100 nodes. The MAC protocols available are the IEEE 802.5 Token Ring /Bus, /CSMA/CD and the proposed protocol. The simulator has a simple user interfaceand can take input either from a terminal or through a data file. The user can specify thetype of source, weather synchronous or asynchronous. The output of the simulator mainlyconsists of the average packet delay at each node, average synchronous and asynchronouspacket delays and the percentage synchronous packet loss for the network; The proposed protocol has been developed by taking into acc out the fact that forsynchronous sources average delay is not as important a performance measure as thesynchronous packet loss probability. Thus it is not necessary to service a synchronouspacket as soon as it arrives. The proposed scheme this idea and services synchronouspacket by sending a special token only if the node is close to time-out. The schemes thusavoid unnecessary token rotations and wastage of bandwidth, the proposed methodimplements a distributed protocol based on the actual requirements of the all the activesynchronous sources. Requires that each node maintain the timing information of all theactive synchronous sources of the network, the protocol essentially operates by followinga set by following a set of rules governing the servicing the synchronous andasynchronous packets based on the value of the Token Sending Time .The TokenSending Time is defined as the time after which only the node closest to time-out shouldtransmit a packet, if packet loss at all other synchronous nodes is to be avoided.Therefore when the system time becomes greater than the token Sending Time isforwarded to the node closest to time-out. Since the value of the Token Sending Timedepends on the expiry time of all the active synchronous sources in the networksynchronous sources will be serviced protocol asynchronous sources are allowed toaccess the network only their transmission can be safely done without adversely protocolhas been compared with that of the IEEE 802.5 Token Ring. It was found that theproposed scheme is able to provide much lower values of average synchronous packetloss probability as compared to an IEEE Token Ring system carrying both synchronousand asynchronous traffic on the same priority and significantly lower both synchronousand asynchronous traffic on the same priority and significantly lower values of averageasynchronous packet deals as compared to an IEEE Token Ring carrying synchronouspacket delay as compared to an IEEE Token Ring carrying synchronous traffic on ahigher priority than asynchronous traffic.

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Title : *Transputer Implementation Of Systolic Arrays*

Author(s) : *Rao M K V Subba*
Roll No : *9010426*
Supervisor(s) : *Prasad Hari*

Abstract

The thesis aims at implementing systolic signal processing algorithms on a transputer array. Matrix multiplication convolution, Fast Fourier transform, sorting and Fast Walsh – Hadamard algorithms are selected for parallelization. The graph based systolizat ion procedure is chosen for deriving systolic algorithms from their sequential versions. The algorithm design phases consist of the selection of projection and scheduling vectors, mapping the computation onto a processor array and problem partitioning. The partitioned algorithms are implemented on 2,4,and 8 trasnputer arrays. All the program coding is done in Occam, the native language for the transputers. The program development, testing and debugging is done under the Transputer Development System environ ment. The performance of the systolic structures is estimated.

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Title	:	*Design And Implementation Of Ds Spread Spectrum Multiple Access System*
Author(s)	:	*Kumar Sanjeev*
Roll No	:	*9010440*
Supervisor(s)	:	*Sinha Vishwanath*

Abstract

Spread spectrum technique with its inherent interference attenuation capability, has ever the years become an increasingly popular technique for use in many different systems. In the present work, we have exploited the multiple access capability of the tec hnique. A code division multiple - access (CDMA) system is not only used in military communications, but it also has varied commercial applications. Direct sequence technique has been chosen to achieve spreading the dispreading the signal. Gold codes were us ed as direct sequences. Two separate transmitters for voice and data were developed. The receiver has been designed using Delay Lock Loop (DLL) technique. Hardware for transmitter was implemented and a software program for studying the performance of DLL r eceiver was developed

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Title : *Transputer Implementation Of Signal Processing Algorithms*

Author(s) : *Shreenivas Galgali*
Roll No : *9010416*
Supervisor(s) : *Siddiqui M U*

Abstract

This thesis aims at implementing some signal processing algorithms on a transputer network. Matrix multiplication convolution, discrete Fourier transform (goertzel algorithm), fast Fourier transform (radix 2, radix 4), fast Walsh - Hadamard transform, two dimensional fast Fourier transform, and two dimensional convolution are selected for parallelization. Parallel algorithms are derived from their sequential versions by using partitioning approach. The parallel algorithms are implemented on a network of 2, 4, 8 transputers. All the program coding is done in Occam, the native language for transputers. The program development, testing and debugging are done in the transputer development system (TDS) environment. The speedup factors and efficiencies of the par allel algorithms are measured for different sizes of input data

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Title : *Studies In Implmentation Of SNMP*

Author(s) : *Bapat Kundan Vijay*
Roll No : *9010410*
Supervisor(s) : *Barua Gautam& Srivathsan K R*

Abstract

Prime objective of network management is sound operation of the network. From the user point of view means an easy access to the network services. Facility to work remotely on a machine. Etc. from the point of view of system administrator, the general heal th of the network is of prime concern. Information on network routing tables, the link - connections, load distribution on the network and a host of other network statistics, have to be collected, to give a global picture for the network operating status. T he "Simple Network Management Protocol (SNMP)" is a standard recommended by the Internet Administrative Board, for networks based on Internet suite of protocols. In this thesis we have attempted an implementation of SNMP on the local LAN, which is based on the Internet suite. SNMP consists of a manager and several agents residing on various machine on the network. The manger queries the agents about various network parameters. Agents retrieve the information from the hosts and return it to the manager. The primary communication primitives of SNMP protocol have been implemented. Manager resides on a MicroVAX. Agent codes provided with 4BSD ISODE package have been installed on UNIX agents MicroVAX and SUN. Minimal agent capabilities are provided on two intern etworking devices, router and bridge

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Title	***:***	***Wavelet Decomposition And Reconstruction Of Images Using Transputer Arrays***
Author(s)	***:***	***Srivastava Anurag***
Roll No	***:***	***9010406***
Supervisor(s)	***:***	***Gupta Sumana***

Abstract

In this thesis, an attempt has been made to study and implement the concepts of Wavelet Transforms and multiresolution approximation of images on a network of Transputers. The decomposition and reconstruction algorithms are derived first for one -dime nsional case and then extended to the two - dimensional case i.e., the case of images. These algorithms are implemented on a linear array of eight transputers using the data -partitioning approach. The performance of Wavelet decomposition and reconstruction o n noise -corrupted images are also studied. All the program coding is done in Occam, the native language for the transputers. The program development, testing and debugging is done under the Transputer Development system environment. The performance of the various basis functions used are compared.

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Title : Pwm -Based Single -Phase Ups

Author(s) : Debnath H C
Roll No : 9010417
Supervisor(s) : Doradla S R

Abstract

The uninterruptible power supply (UPS) is an integral and indispensable part of the supply system for many critical loads. In this thesis, a single - phase on - lines UPS is designed and developed to meet given specifications. High frequency sinusoidal PWM swi tching strategy is adopted for the inverter system. The experimental study shows good sinusoidal output voltage. The high switching frequency allows smaller filter components. The closed - loop response is also carried out with step changes in the load circu its

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Title : ***Implementation Of LPC Based Speech Processing Algorithms On Adsp 2100***

Author(s) : ***Pandey Peeyush***

Roll No : ***9010429***

Supervisor(s) : ***Siddiqui M U***

Abstract

This thesis aims at implementing some f the speech processing algorithms, which can be used as central building blocks for the development of a speech processing system based around the ADSP 2100 DSP microprocessor. Code excited linear prediction (CELP) , pole - zero analysis, and formant based analysis with pattern matching of voice on the frequency axis are the algorithms that have been implemented. The CELP algorithm forms the main unit of a coder - decoder. The pole - zero analysis forms the central unite f or a speech recognition system and the pattern matching algorithm forms the basic unite for a speaker verification/identification system. The program development, testing and debugging has been done on the ADSP 2100 simulator and algorithm have been implem ented on the ADSP 2100 evaluation board and comparisons have been made with the implementation in a high level language "C". Suitability of the implementations for real time cases has been discussed.

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Title : *Representation And Identification Of Alpha-Numeric Characters Using Galois Transform*

Author(s) : *Gupta Alok*
Roll No : *9010403*
Supervisor(s) : *Siddiqui M U*

Abstract

We obtain two dimensional Galois transform representation of different image sizes. Calculation of Galois transform coefficients has been carried out by using FFT, systolic array and Horner's rule. Four T414 Transputers and five T800 Transputers have been used in linear and mesh configuration for this purpose. Various algorithms are evaluated by comparing sequential, parallel one node and parallel 8 node timings for different image sizes. As a concrete application, FFT based configuration with mesh connecte d processors is used to calculate Galois coefficients for IBM font of English alphabet and Arabic numerals. The coefficients are used to identify these characters by comparing them with coefficients stored in computer memory. Two algorithms have been imple mented for this purpose. Their performance is compared to that of a straight sample domain algorithm in terms of the average number of comparisons required for identification in each case.

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Title : Modelling And Recognition Of Eeg Signals
Author(s) : Bhattacharya Puranjoy
Roll No : 9110432
Supervisor(s) : Sharma Govind

Abstract

The EEG signal is a no stationary random signal. However, under the assumption ofpseudostionarity, it is possible to model it parametrically over sufficiently short intervals.the parametric signal space may be partitioned into a collection of labeled event classes,each class being characterized by a representative parametric model. Then aparameterized by a representative parametric model. Then a parameterized by arepresentative parametric model. Then a parameterized segment of EEG data may beclassified as on of these events depending on which representative model has maximumproximity. Once the entire signal is expressed as a sequence of labeled events, a HiddenMarkov Model is used to record and to reproduce the succession properties. This modelassumes that there is an underlying Markovian state space, which is invisible, while theoutcomes are probabilistic functions of the states concerned. The recognition problemrequires that if an observation sequence is given, the model should be able to output thesequence of states most likely to have been responsible for generating it . An application for this model has been sought to be found in medicaldignostics. Aspart of the modeling exercise, the Markovian state space has been merged to alocalization model of brain functioning. With this visualization, it is expected that themodel be output sequence of states will reflect the physical health of the patient

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Title : *A Simulator For Microcoded Signal Processors*

Author(s) : *Visweswar J*
Roll No : *9010420*
Supervisor(s) : *Mahanta Anil*

Abstract

Microcoded systems are used extensively in signal processing applications. They attain high functional parallelism and thereby achieve high throughput. Simulation of a system is a software tool widely used for the system. Development and checking. In this thesis, a number of microcoded signal processors are proposed and a simulator for these systems is developed. The simulator permits programs to be finely - tuned in software prior to making significant effort to bring up the target system in hardware. The s imulator is interactive, it allows display of registers and memory contents. Single and full - speed run is possible. Using this simulator performance of the proposed microcoded systems is evaluated with a few DSP algorithms

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Title : ***PC Based Simulation Of Digital Communication System***

Author(s) : ***Das B Anand***
Roll No : ***9010409***
Supervisor(s) : ***Mahanta Anil***

Abstract

A software environment for analysis and simulation of Digital Communication system is discussed. This software package offers the signal processing capabilities on the digital data and provides an environment for simulation and analysis of a Digital Commu nication System. User can generate different types of Digital/Random Data sequences or can read from already stored data from Disk Files, process in block of data sequences as desired and store the results on Disk Files for later use. User can signal proce ss the data in a number of available standard ways : at the Functional Block Level, at collective Block Level, or at the TOTAL SYSTEM level. Here the System is divided into a number of convenient Functional Blocks for easy Simulation and for study and ana lysis

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Title : Design Of A Digital Microwave Los Link

Author(s) : Srivastava Puneet
Roll No : 9020406
Supervisor(s) : Sachidananda M

Abstract

The design of a digital microwave LOS link at 18 GHz frequency band is described in this thesis. Digital signal, QPSK modulated at IF is available. The design includes selection of proper frequency for two way communication. Transmitted power, in the prese nce of noise and fading, for proper detection of QPSK signal at the receiver output, is calculated. In this thesis, design of the transmitter and the receiver for RF signal is given. In the transmitter, the IF is upconverted to RF and amplified to a prope r power level. In the receiver, the RF is downconverted to IF for detection of QPSK signal. Various circuits required in the transmitter and receiver are designed in this thesis. The transmitter and receiver circuits are designed either on a microstripline or on a suspended stripline. A computer program is written for the design of these circuits. The program gives coordinate points for the layout mask of the circuit. The layout mask the circuits required in the transmitter and receiver are obtained from th e program and shown in this thesis. After the design of various circuits, they are integrated in one block. A test filter at X - band of frequency is fabricated and its performance is studied.

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Title : *A Programmable Interface Unit For A Systolic Array*

Author(s) : *ThyagarajanT S*
Roll No : *9010452*
Supervisor(s) : *Mahanta Anil*

Abstract

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Title : *Analysis Of Probe Fed Waveguide Slot*

Author(s) : *Sivadas Apu*
Roll No : *9110405*
Supervisor(s) : *Sachidananda M*

Abstract

of a small dipole or a loop kept within the waveguide. The dipole (loop) is supported on a pair of transmission lines attached to the slot. The specific placement of the wires with respect to the slot, leads to a simple analytical formulation, based on the method of moments and transmission line theory. The theoretical conclusions are validated

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Title	***:***	***Microcontroller Based Two-Tier Controller For Parallel Control***
Author(s)	***:***	***Shashidhara B P***
Roll No	***:***	***9010411***
Supervisor(s)	***:***	***Ghosh Arindam***

Abstract

A two - tier controller with a PC as the front - end computer and a microcontroller acting as slave to the PC for actual interaction with the sensors and actuators has been studied. The design exploits the capability of the microcontroller to efficiently inter act, in a time shared manner, with many control systems having different control configurations such as potentiometers, encoders for sensing and DC motors or stepper motors for actuation, thus achieving parallel control. The inability of the microcontrolle rs to perform floating -point computations is compensated by the PC. The two together are able to control efficiently a complex control system. The design permits the user to programme a path profile of his choice through the PC. As the front end of the sys tem is a PC, flexibility and user friendliness are built into the system. A microcontroller evaluation module has been used to demonstrate the simultaneous closed loop control of two DC motors. Each motor has been tested for the control system's ability to execute a programmed speed profile in the closed loop. Experiments have shown the basic feasibility of the architecture and design for achieving parallel control

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Title : Easily Testable PLA-Based Finite State Machines

Author(s) : Prakash B
Roll No : 8910430
Supervisor(s) : Hasan Mohammad Mozaffarul

Abstract

The present work addresses the problems of synthesis and testing of easily testable PLA -based finite state machines (FSM). A new system named FISTEM, for testability synthesis and test generation of PLA - based FSMs is proposed. A nonscan desig n methodology based on constrained state assignment and logic optimization, is used which guarantees testability for all combination ally irredundant crosspoint faults in the PLA. State assignment technique used, which originally proposed for multilevel lo gic implementation is shown to be effective in minimizing the number of product terms in an optimized PLA implementation. Effect of single crosspoint defects in programmable arrays on their input - output relations has been studied and the necessary co nstraints required for testability synthesis of a PLA -based Moore or mealy finite state machine have been formulated. FISTEM makes use of the logic minimization program ESPRESSO to obtain optimized, prime and irredundant two - level covers for output logic (OL) and next state logic (NSL) functions of the FSMs. Test sequences for all the testable crosspoint faults are obtained combinational test generating techniques alone. An exact algorithm is used for this to obtain maximum fault coverage. Some power ful heuristics in the area of back end fault simulation and “don’t -care” bit fixing are also used in the program for test set minimality. For most of the state machine examples considered, the system works very efficiently to produce an optimized ea sily testable PLA - based logic implementation and a compact set of test sequences to cover all the irredundant faults in the PLA. These results show that the area overhead in return for easy testability is small.

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Title : ***Line Current Based Condition Monitoring Of Electric Drives***

Author(s) : ***Dhar Ashutosh***

Roll No : ***9010401***

Supervisor(s) : ***Srivastava S C& Kalra Prem Kumar***

Abstract

The aim of condition monitoring is to recognize the development of a defect in the machine well before it amplifies into a failure, by continuously evaluating its health, based on certain monitored parameters. This thesis presents an extensive review of co ndition monitoring techniques based on mechanical, chemical and electrical methods as applicable to motor drive system. An attempt has been made to exploit the potential of line current based condition monitoring using an experimental set up in the laborat ory. In doing so the stress was emphasized on determination of the suitability and effectiveness of various signal processing techniques like statistical analysis, frequency domain analysis, linear predictive analysis and cepstrum analysis to reliably dete ct and identify various defective conditions. A comparison of the results obtained using the above signal processing techniques clearly indicates the emergence of Ceptrum Analysis as the most effective technique to be used in conjunction with line current based condition monitoring of motor drive system.

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Title : Design And Simulation Of Analog Digital Asic
Author(s) : Kumar Subodh
Roll No : 9010447
Supervisor(s) : Hasan Mohammad Mozaffarul

Abstract

The work is aimed at designing, simulating and creating the layout of a Digital Voltmeter (DVM) chip in 2 micron CMOS technology as an example of Application Specific Integrated Circuit (ASIC). Various analog and digital building blocks to be used in the D VM chip are designed and simulated using SPICE to meet the required specifications. The layout has been created by using layout editor DALI of the NELSIS IC Design System. The leaf cells have been synthesized to realize the higher level building blocks. Th e chip, as a whole. Could not be simulated on MicroVAX due to inability of the system to handle the large complexity of the chip. The performance of the chip has been estimated from its building blocks. The whole circuit would approximately occupy a silico n chip area of 4 mm 2 . the chip is expected to operate with ± 5 V power supply. The expected value of accuracy is within ± 0.2 percent. The power dissipation in the chip is estimated to be less than 20 MW

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Title : *High Density PWM Dc-Ac Power Converter Using High Frequency Link For Utility Load Interface*

Author(s) : *Anandan M*
Roll No : *9010422*
Supervisor(s) : *Dubey G K*

Abstract

The present work involves the development of a high density DC to AC power conversion system that can be used as a utility load interface system. An attempt has been made to eliminate the bulky low frequency transformer stage which is used in a conventiona l DC to AC power conversion system thereby increasing the power - per - unit - mass volume of the converter system. This has been done by using a front end boost converter to step up the incoming DC voltage and then using a PWM inverter stage to get the required output AC voltage. An experimental unit has been designed and constructed and observations have been reported.

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Title	***:***	***On Line Protection Of Induction Motor Using Microprocessor (8085)***
Author(s)	***:***	***Tiwari Ashok***
Roll No	***:***	***9010408***
Supervisor(s)	***:***	***Singh L P***

Abstract

Microprocessor based relaying in an important area of research for motor protection. The continual increase in use of motors particularly induction motors in industries has in turn resulted in requirement of very reliable and efficient operations of these motors. The economic efficiency, reliability and other considerations have necessitated the development of a fast, reliable and efficient protection scheme, which can ensure the motor security and reliability. With the advances in integrated circuit techno logy. It has become possible to develop a microprocessor based relaying scheme for the protection of industrial motors. It is in this context, that on line protection of industrial motors using microprocessors have a great potential in future. In this ref erence, the present thesis aims to develop a microprocessor based relaying scheme for the protection of induction motor. Sample signals are taken to simulate faults and thus establishing the feasibility of the proposed protection scheme.

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Title : ***Optimal Design Of PLA-Based FSMS***

Author(s) : ***Raman S***

Roll No : ***9010441***

Supervisor(s) : ***Hasan Mohammad Mozaffarul***

Abstract

This work addresses the problem of optimal design of PLA based finite State Machines. State assignment profoundly affects the area, delay and testability of the combinational component of the FSM. Optimal design is aimed at minimizing the area of the PLA i mplementing the combinational component of the FSM. All previous approaches for PLA based FSM synthesis use symbolic minimization and solve this problem as an encoding problem. These approaches use greater than minimum code length and hence results in high er area counts. The present work deals with state assignment algorithms that use minimum code length for encoding the symbolic states of the FSM. These algorithms attempt to maximize the size and frequency of occurrence of the common cubes in the encoded machine prior to optimization. These algorithms encode the states based on the proximity relations in the Boolean space. Some methods to combine the various algorithms are also presented. Certain important optimality rules are specified. The delay in the P LA and the size of the test set are also determined. The effect of the algorithms on the area of the decomposed PLA are analyzed. The algorithms were tested on a set of MCNC FSM benchmarks and the results are compared. The PLAs were tested for delay, test vector size and area after decomposition. The results show that the algorithms explained, compare favorably with symbolic minimization based approaches. Area count improvement were found to vary as much as 30% in some cases.

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Title : *Analysis And Simulation Of Power Mosfets*

Author(s) : *Gupta Vandana*
Roll No : *9010453*
Supervisor(s) : *Hasan Mohammad Mozaffarul*

Abstract

In this work, a detailed theoretical analysis of the important device parameters like on - resistance, device Tran conductance, cell structure and high frequency operation of vertical double diffused MOSFET (VDMOD) and insulated gate bipolar transistor (I GT) power devices has been carried out. An analytical model based on the device structure has been proposed. A numerical model for the one dimensional pn junction based on the finite element method has been developed. Since the on - resistance of any semicon ductor determines its maximum current rating, therefore, it is an important device parameter. A two dimensional model based on the finite element method to calculate the on - resistance has been developed. The FEM provides an efficient technique to simulate the behavior of semiconductor structures, which involve curved boundaries. Results have been presented for VDMOS and IGT power devices

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Title : Digital Protection Of A Synchronous Generator
Author(s) : Baig Istikhar
Roll No : 9010419
Supervisor(s) : Singh L P

Abstract

As the power system is expanding, the problem of protection of the power system has become a challenging task for the power system engineers. The problem of protection of synchronous generators against all abnormal conditions has been of great conce rn to the protection engineers because the synchronous generator is the very source of power. If the faulty synchronous generator is not isolated quickly and reliably, the entire power system may get disturbed; at the same time, if healthy synchronous gene rator is isolated then also the power system will be disturbed because of mismatch between generator and the connected load. Therefore, it is essential that the relay be reliable, efficient and quick in operation. Electromechanical relay is the olde st type of relay, however, it has some limitations to meet some basic features like reliability, speed selectivity simplicity and economy. Static relay almost revolutionarised the protective relaying scheme but they have some limitations. Development of mi croprocessors has made feasible 'DIGITAL RELAY', digital relay satisfies all the above features and also it self checking features and flexibility are unique. The digital relay developed is based on microprocessors 8085, it is needs to check input sign als of incoming, outgoing current and field current, and sends trip command if the fault is detected. The relay takes only five milliseconds of processing time. Software is developed with the help of microprocessor 8085 simulator and tested for diffe rent waveforms of input signals and has performed satisfactorily. Hardware is developed with minimum chips using workstation available in the microprocessor laboratory. Digital filters are used to overcome some of the drawbacks of analogy filters. The prop osed microprocessor based relaying scheme for the synchronous generator has been designed, fabricated and tested and its performance is found to be very satisfactory.

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Title : *Fast Algorithm For Voltage Contingency Selection*

Author(s) : *Rao M Venkateswara*
Roll No : *9020404*
Supervisor(s) : *Srivastava S C& Kalra Prem Kumar*

Abstract

This thesis is addressed to the development of fast and efficient methods for voltage contingency selection. One of the problems faced in the real time execution of security analysis, especially the voltage security analysis, is the non - availability of fast and accurate methods for predicting the post outage conditions. Hence, the attempts have been made in this thesis to suggest a new set of voltage and reactive power distribution factors which can be used for rapid computation of the post outage syste m states with sufficient accuracy. Another difficulty is due to non - availability of proper performance indices which will reflect the true relative severities of contingencies. Various contingency ranking methods available in literature, in general , suffer from the masking and misranking effects. To overcome these problems, several new higher order performance indices have been explored. A simple approach, based on least square errors minimization, to compute the optimal values of weights associated with voltage and reactive power performance indices has been suggested. The potential of the proposed distribution factor based model and the new performance indices for voltage contingency selection have been tested on IEEE - 14 bus and a 19 bus Indi an system.

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Title : *Study Of Robustness Of Optimal Digital Controller With A Prescribed Degree Of Stability*

Author(s) : *Tamhankar M V*
Roll No : *9010451*
Supervisor(s) : *Hole K E*

Abstract

The robustness properties of discrete time linear quadratic regulator are studied. The return difference equality for a discrete time linear quadratic regulator with a prescribed degree of stability is achieved. It is found that the guaranteed stability ma rgins achieved reduce as the degree of stability is increased. It is shown that the stability margins achieved are a measure of nearness of the closed loop poles to a circle which is interior to the unit circle on the z - plane. Systems with lesser degree of stability, are shown to possess these guaranteed stability margins

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Title : *Design Of Robust Controller For A BTT Missile*

Author(s) : *Das Anil Kumar*
Roll No : *9010404*
Supervisor(s) : *Hole K E*

Abstract

The robustness to parameter variations uncertainties and disturbances is an integral partof any good practical controller-design and should be achieved wherever possible. Thecapability of a controller to maintain system stability without compromising itsperformance become a critical issue when three is fast variations in parameters in amaneuvering system like a missile following a moving target. In this thesis, a robust controller for a Bank-To-Turn missile is designed using thetheory of Linear Quadratic Regulator with a prescribed degree of stability. The homingphase of the missile-flight is considered when the missile has to make fast maneuvers tokeep it pointing to the equally “clever” target. Sufficient conditions are started whichwhen satisfied guarantee the optimality of the controller for structured uncertainties in thesystem state and input matrices. The roll, pitch and yaw control loop frequency-responsesof the missile are obtained to get the stability margins for the different control loops. Thefrequency-domain performance of the missile, while using the designed robust controller,is compared with the performance of the same missile when it uses a controller in theliterature.

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Title	***:***	***Solar - Powered Battery - Operated Electric Vehicle***
Author(s)	***:***	***Bhatiya Shekhar Sharan***
Roll No	***:***	***9010442***
Supervisor(s)	***:***	***Dubey G K***

Abstract

Battery-operated electric vehicle (BEV) offers an easy to control, fuel efficient andpollution free transport. In countries like India which are dependent on the other countriesfor the petroleum, future of the most of the transportation systems lies in the BEV. In thepresent work, expressions based in the vehicle dynamics are developed to determinetorque and power requirements of the BEV drive. Accordingly solar power and batteryrequirements are described. To achieve power efficient operation of expensive solarpower, battery charging from photo-voltaic array through a maximum power pointtracker (MPT) circuit is experimentally tested and described. Generally dc series motorsare used in EVs. The brushes and commutator require frequent replacement andmaintenance. To overcome these problems, IM variable frequency drive is proposed. APUM-VSI operating at high switching frequency is employed to obtain variable inverteroutput voltage with low harmonic distortion. A new PWM algorithms suitable for non-constant voltage source which calculates pulse durations in real time is described andexperimentally tested. Since the widths of the pulses are computed on-line using singlechip microcomputer, storage requirement is minimal as well as hardware and softwareare very compact. Prototype hardware and software is developed on in-circuit-emulator.The system is capable of controlling IM drive satisfactorily over a frequency range of 5to 50 Hz

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Title : ***Robustness Properties Of An Optimal Pi Controller***

Author(s) : ***Tomar Yashpal Singh***

Roll No : ***9010459***

Supervisor(s) : ***Hole K E***

Abstract

A method of designing an optimal PI controller is discussed. The stability robustness and optimality of the system using the optimal PI controller are discussed. The stability robustness is expressed in terms of the gain margin and phase margin, and in te rms of bounds on system uncertainties which will preserve the stability of the perturbed closed loop system. The optimality robustness is expressed in terms of bounds on the perturbation in the system matrices such that the optimally of the closed loop sys tem is preserved. Some numerical examples are solved to illustrate the results.

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Title	***:***	***Investigation Of Insulating Properties Of Low Vacuum In Extremely Non-Uniform Field Configurations By Ac Power Frequency Voltage***
Author(s)	***:***	***Agrawal Manish Kumar***
Roll No	***:***	***9010443***
Supervisor(s)	***:***	***Arora Ravindra***

Abstract

Corona or stable partial discharge in gaseous diselectrics occur under extremely non -uniform field conditions. This leads to a deterioration in the insulating properties of gases. In this thesis measurements have been made on the corona inception voltage and breakdown voltage of air in the low vacuum range of pressures upto 1 Torr under Different electrode configurations. The electrode configurations are point – sphere (3 cm and 5 cm gaps), and small sphere – large sphere (3.7 cm ga). All the three configur ations produce extremely non - uniform fields. A pressure vessel has been used in this work to enclose the electrodes and to make measurements at different pressure. It had a transparent cover to allow visual inspection of glow and breakdown. Measuremen ts have also been made for the conduction currents. However, these found to be measurable only under glow - discharge conditions around 1 Torr pressure.

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Title	***:***	***Control Of Dynamic Interaction In A Power System Having Muliple Static VAR Systems***
Author(s)	***:***	***Sinha Ved Prakash***
Roll No	***:***	***9020409***
Supervisor(s)	***:***	***Varma Rajiv K& Sachchidanand***

Abstract

In this thesis the study of dynamic interaction between various dynamic devices of a large power system having multiple static VAR systems has been carried out. Also a systematic procedure has been established to mitigate any adverse interaction through de sign of damping control in the form of power system stabilizer on generator and auxiliary control of static VAR compensators. The damping control design is based on eigenvalue analysis technique and uses information regarding state and voltage participatio n factors, observability factor, mode shape in selecting a suitable site for placement of damping control and the choice of potential feedback signal.

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Title	***:***	***Prediction Of Voltage Stability And Stability Margin In Radial Systems***
Author(s)	***:***	***Gupta Rajeev Kumar***
Roll No	***:***	***9010433***
Supervisor(s)	***:***	***Kalra Prem Kumar***

Abstract

Voltage instability in a power system network is generally attributed to the reactive power deficit caused increased system loading, network or power outages or transformer tap changing. Radial voltage instability is defined as a situation when the load ing on a radial network exceeds the lines capability to control the receiving end voltage. Most of the literature on study of radial voltage instability phenomenon have considered simple single section radial networks. In this thesis an attempt has b een made to analyze the phenomenon of voltage collapse for practical radial power system networks, which consists of multiple section with different R/x ratio and load tapped from each section through the transformers. Furthermore the effect of various typ es of load modeling e.g. constant power type and generalized or voltage dependent load and the reverse action of tap changing have been studied. Further in literature a very little effort has been made in suggesting a simple and fast approach useful t o operators in circumventing this unwanted situation or predicting the stability margin and control actions. In this thesis generalized performance charts have been suggested, which can be used by to the operator for fast prediction of voltage stability ma rgin and deciding the required control actions for any size and complexity of radial network. A method of finding out the single section equivalent of the complex radial networks having multiple, non -uniform sections, load tappings through transforme rs and generalized voltage dependent loads have also been described in this thesis. The above studies have been demonstrated on two practical radial system networks

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Title	***:***	***Investigation Of Insulating Properties Of Low Vacuum In Weakly Non-Uniform Fields For Ac Power Frequency And Switching Impulse Voltages***
Author(s)	***:***	***Gupta Shyam Sunder***
Roll No	***:***	***9010445***
Supervisor(s)	***:***	***Arora Ravindra***

Abstract

In weakly non - uniform fields, no stable partial discharge precedes the breakdown of the dielectric. In this work, insulation properties of low vacuum (pressures from 760 Torr to 1 Torr) under two different electrode configurations used for the ex periments are sphere - sphere (φ - 5cm) gap and small sphere - large sphere (φ1 - 2 cm; φ2 - 5 cm) gap. As the pressure is reduced from atmospheric pressure to 1 Torr, the breakdown strength gradually decreases. At 1 Torr pressure, breakdown strength is very small conduction currents of the order of tens of mA were measured under the glow discharge conditions around 1 Torr pressure

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