M.TECH. THESIS ABSTRACTS 2001

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Microelectronics, VLSI & Display Technology

RF Microwaves& Photonics

1	Studies On Diffused Indoor Optical Wireless Systems	John Joseph	18
2	Design And Implementation Of An Outdoor High-Speed Optical Wireless Link	John Joseph	19
3	A Wide Band Mm-Wave Triplexer In Suspended Stripline	Sachidananda M	20
4	Design And Implementation Of IRDA Compatable Point To Point Optical Wireless Link For Indoor Applications	JohnJoseph	21

Signal Processing, Communications & Networks

Power and Control

Title : VLSI Implementation Of Discrete Wavelet Transform
Author(s) : Vivek T D
Supervisor(s) : Mazhari Baquer
Roll No : 9910488

Abstract:

The discrete wavelet transform (DWT) is one of the important tools for signal processing. Real time computation of the DWT often requires dedicated VLSI implementations. In this thesis, the design of a VLSI circuit that computes DWT of a sequence of input samples using 6 - tap filters for 3 stages of wavelet decomposition is described. The circuit was designed stating with a behavioral model and passing through register - transfer logic, gate, and physical design levels of the VLSI design flow. A hierarchical d esign methodology was adopted for RTL level design and logic synthesis, and a standard cell approach was followed for physical design. The VLSI DWT circuit has an area of 10 mm 2 and can operate at a maximum speed of 40 MHz under typical operating condition s. At this speed, the VLSI circuit can process colour frames of video signals in real time.

For more details click here **back**

Title : Signal Processor For Ac Plasma Display Panel
Author(s) : Puvvada Naga Satya Srikanth
Supervisor(s) : Sharan R
Roll No : 9910452

Abstract:

AC plasma display panel has great potential in commercial color display applications because of its large screen area, compactness, less weight, etc. the format of data required for plasma display panel is very different from that required for CRT so that a converter is required in-order to display RGB signals of CRT on a plasma display panel. To carry out this transformation a signal-processing chip for 640X480 resolution AC plasma display panel has been developed. The full chip is designed such that it can be partitioned into 12 different commonly available FPGs easily. Its complexity is about 30 thousand gates and can work up to 30MHz frequency if implemented on a FPGA

For more details click here **back**

Title : *Analytical Modelling Of Subthreshold Behaviour For Submicron Mosfets*

Author(s) : *Kesri Ambrish Kumar*
Supervisor(s) : *Qureshi Shafi*
Roll No : *9910408*

Abstract:

In this thesis, new models for threshold voltage and subthreshold current are presented, which are applicable for both short - channel and long - channel MOSFET devices. In this work, the surface potential variation along the channel has been investigated for the location of minimum surface potential. The minimum surface potential is used to determine the threshold voltage for the long and short - channel devices. Further, analytical expression for the subthreshold current has been obtained by using the minimum s urface potential. The results are compared for the channel lengths ranged from 0.13 µm to the 2.0 µm with those obtained by MINIMOS 6.1 (2 - dimensional devices simulator) and are in good agreement for the gate lengths of 0.13 µm to the 0.5 µm. The variatio n of the electrostatic potential toward the substrate, from the surface, at the point of minimum surface potential is also presented. This potential decreases rapidly from the surface toward the depth. Maximum electrostatic potential, for the n - channel MOS FET having gate voltage above the flat - band voltage, occurs at the surface and hence, inversion of channel is maximum at the surface and decreases rapidly toward the depth. This is why subthreshold current is basically surface - leakage current. For short -channel devices, decrease in gate length not only causes tremendous increase in this electrostatic potential distribution but also increase in depletion layer width. For long -channel devices the dependency of this electrostatic potential on the gate length i s not reported. The threshold voltage and subthreshold current are calculated at the point of minimum surface potential. The model presented by us for threshold voltage predicts that for short -channel devices the threshold voltage is also the function of the location, where minimum surface potential occurs. Threshold voltage shows significant dependency on the drain voltage for the smaller gate lengths. Reduction in gate length caused reduction in the threshold voltage for short - channel devices. The effect ive threshold voltage can be dropped to zero or negative with further decrease in gate length. The drain voltage lowers the energy barrier of electrons. This phenomenon is known as Drain - Induced Barrier Lowering (DIBL). The model predicts that DIBL is inve rsely related with the exponential function of gate length and hence, for long - channel devices DIBL has no significance but as we decrease the gate length, the effect of DIBL increases exponentially. We compared our threshold voltage model with the device simulator program MINIMOS 6.1, which is applicable up to minimum gate length of 0.1 µm, and got nearly same relationships for both small and large - gate lengths. We introduced only two fitting parameters, in our model, on to show the effect of drain voltag e on the depletion layer width and other to account the effect of drain voltage on the inversion charge and

hence, on the subthreshold current. The calculated results of subthreshold current are also compared with the experimental results for same device p arameters. Calculated results are in close agreement with the experimental results. And, in last we would like to mention that the presented models are very simple and are easy to understand. For gate lengths less than 2.0 μm and larger than 0.13 μm (0.13 μm ≤ L ≤ 2.0 μm), the presented subthreshold current model predicts good agreement with the simulated results even for smaller gate voltages (V GS ≤ 0.25 V) but the validity of our model may be questioned for larger gate lengths (L > 2.0 μm) and for very small gate voltages (V GS ≤ 0.25 V), when L > 2.0 μm. the models spend very less time in computation in comparison to time taken by MINIMOS 6.1, for same analysis.

For more details click here **back**

Title : *Parametric Optimization Of Analog Circuits Using Neural Networks*

Author(s) : *Dutta Aloke*
Supervisor(s) : *Basu Arghajit*
Roll No : *9910415*

Abstract:

Owing to the increase in the number of new application specific integrated circuit (ASIC) designs that include complex analog functions, the need for computer aided design (CAD) tools for analog circuits is being increasingly felt. In the work, we present a new design automation strategy that can fully automate the design with path starting from the performance specifications and ending at a sized circuit schematic. This strategy relies on the radial basis function (RDF) network to predict the circuit performance from the design variables, and the penalty function method to solve a constrained optimization formulation of the synthesis problem of the circuit. In our method we do not need to formulate circuit equations in order to get the performance of the circuit from the design variables-another RBF network is also used in order to generate the initial values of the design variables from the given performance specifications. A database is created using SPICE for each topology, in order to train both the RBF networks. Using this approach, some of the basic circuit topologies in MOS technology are optimized, e.g., current sources (simple, cascode, and Wilson) and a common-source amplifier as a gain stage. The design routines for two basic CMOS op-amp topologies, e.g., the simple operational Tran conductance amplifier (OTA) and the basic compensated three-stage operational amplifier have been developed in this work. Once the optimization is done the program creates an output file to store the design variables, which can be used in SPICE simulation to compare the results with the given performance specifications. The design results obtained from our parametric optimization program of the circuit variables matched reasonably well those obtained from SPICE simulation for each of the topologies designed in this work.

For more details click here **back**

Title : *A Hierarchical Approach To Topology Generation Of Analog Circuits*

Author(s) : *Sur Rajarshi*

Supervisor(s) : *Mazhari Baquer*

Roll No : *9910467*

Abstract:

The present work describes a hierarchically structured framework for analog circuit synthesis. The analog circuit topologies are represented as a hierarchy of templates of abstract functional sub blocks, each with associated detailed design knowledge. Init ially, a particular topology to be designed is selected at the top most level of the hierarchy. This is followed by a design phase where the input specification are translated from the top most level in the hierarchy to the next lower, more concrete level. Genetic Algorithm based optimization is used during this translation process to obtain the new optimized set of specifications for each of the building sub blocks. The specifications obtained for each sub block are divided into two sets S0 and S1. One sub set of the specs (S0) along with the choice of topology is used to generate a new value for the other subset S1'. Depending on the match between the elements of S1 and S1' the topology is considered a success or a failure. The final topology is selected fr om among the successful topologies using a suitable figure of merit. The validity of this approach is demonstrated by designing several kinds of 2 stages Miller Compensated op amp which is an affixed connection of different building sub blocks such as load current mirrors, differential pairs, bias current mirrors and trans conductance amplifiers. Detailed SPICE simulations are then performed to verify the results obtained

For more details click here **back**

Title : *Design Of A First Order Sigma -Delta Modulator*
Author(s) : *Nigam Sachin*
Supervisor(s) : *MazhariBaquer*
Roll No : *9910471*

Abstract:

The emergence of powerful digital signal processors implemented in CMOS VLSI technology creates the need for high - resolution analog – to digital (A/D) converters that can be used as an interface between the digital and the analog world. A/D converters based on Sigma - delta modulation combine sampling at rates well above the Nyquist rate with negative feedback and digital filtering for achieving higher resolution. In this thesis, we have presented the design of a first order sigma - delta modulator. These conver ters are especially insensitive to circuit imperfections and circuit mismatch since they employ only a simple two - level quantizer, and that quantizer is embedded within a feedback loop. Thus, they avoid the difficulty of implementing complex precision anal og circuits. Oversampling reduces the quantisation noise power in the signal band by spreading it over a bandwidth much larger than the signal band. It is left for digital processing to further reduce the noise.

For more details click here **back**

Title : Design Of Plasma Display Panel Sequence Controller
Author(s) : KumarKuldeep
Supervisor(s) : Mazhari Baquer
Roll No : 9910446

Abstract:

High voltage drivers constitute a significant fraction of conventional 3 -electrode surface discharge type AC - Plasma Display Panel (PDP) cost. The addressing scheme used in a PDP can have a major impact on its cost as it determines the number of such driver s needed. The choice of a suitable addressing scheme has be determined not only with respect to its impact on the number of drivers but also on the relative ease or difficulty of its implementation. With this perspective, the design of a controller for imp lementing a commonly used addressing scheme for a PDP with a resolution of 640x480 (VGA) was undertaken. The design includes a scheme for reducing dynamic false contours, a problem common in PDP. Keeping in mind the rapid advances being made in this field, the design was carried out such that it could be easily adapted to different resolutions or different timing requirements of other addressing schemes. The controller was designed and implemented using FPGA design flow to facilitate future modifications to design. The results from the design indicate that the complexity of controller is not high and timing requirements of a TV frame can be easily met. The chip is small enough to be easily implemented in a commonly available FPGA

For more details click here **back**

Title	***:***	***A New Step To Explore The Moderate Inversion Region For Short Channel Mosfets: Unified Mobility And Drain Current Models And An Improved Threshold Voltage Model Along With Its Extraction Procedure***
Author(s)	***:***	***Mahapatra Santanu***
Supervisor(s)	***:***	***Dutta Aloke***
Roll No	***:***	***9910473***

Abstract:

A semi - empirical unified mobility model dedicated to the modeling of short channel length MOSFETs for low power analog applications has been developed in this work. The existing BSIM mobility model is taken up and modified here in order to incorporat e the coulomb scattering effect, which plays the dominant role in determining the effective mobility of the channel electrons in the moderate inversion region. Using the proposed mobility model, a new drain current model for the quick calculation of the dr ain current in the moderate inversion region has also been developed in this work. In addition to this, a new unified drain current model valid for all the three regions (i.e., the weak inversion, the moderate inversion, and the strong inversion) is presen ted in this work. Results obtained from the proposed model have been verified with the experimental data reported in the literature for 0.26 µm and 0.09 µm channel length MOSFETs which show a perfect match between the experimental data and the simulated mo del characteristics. Another important issue for the low - power - analog - IC applications is the proper modeling and extraction of the device threshold voltage parameter. In this work, a new model for the threshold voltage at the 'onset of the moderate inversion region' along with its extraction procedure have been proposed. The development of this extraction method is based on two new integral functions V x and I x proposed in this work which are insensitive to the drain and source series resistance of th e device and the experimental noise error. The results obtained from the proposed model are compared with the recently reported experimental data for 0.26 µm and 0.09 µm channel length devices and its reliability (i.e., short and narrow channel effects, an d the parasitic series resistance effect of the proposed extraction method) is also tested and compared with the other existing methods by means of the AIM -SPICE circuit simulator. The results reveal that the determined threshold voltage values always meet the 'onset of the moderate inversion region' condition, and that, this extraction procedure is insensitive to the drain source parasitic series resistance and the noise introduced during measurements

For more details click here **back**

Title : Studies On Diffused Indoor Optical Wireless Systems
Author(s) : Janardhan, N
Supervisor(s) : JohnJoseph
Roll No : 9910453

Abstract:

Wireless Infrared (IR) communication systems are being used extensively because of their portability and low cost. In this thesis an attempt has been made to study Diffused Indoor Optical Wireless Systems. A diffused indoor link has been designed using LED as the source and PIN photodetector as the detector. Some simple theoretical models have been suggested to predict the optical power at a given point along the axis of the source. An experimental IR link was implemented using single LEDs and also using an array of LEDs. Sources were characterized and their far - field patterns were measured. These patterns were fitted to the suggested theoretical models. Variation of optical power along the axis of the sources were measured and then compared with theory. Th e experimental indoor link had a data rate 200 kBits/sec and it achieved a range of 8cm using single LEDs and 20cm using multiple LEDs

For more details click here **back**

Title : ***Design And Implementation Of An Outdoor High-Speed Optical Wireless Link***

Author(s) : ***Thomas Saju***

Supervisor(s) : ***John Joseph***

Roll No : ***Y010445***

Abstract:

Free space optical communication is a cost effective, high - bandwidth, wireless alternative for the last mile connectivity of high - speed data to the user premises. The theses deals with the design issues and implementation details of a high - speed outdoor optical wireless link. A detailed review of related work in this field has been done. Various considerations in the design of an outdoor optical wireless links are discussed. An experimental outdoor high - speed optical wireless link with 20 Mbps data rate a nd a link length of 20 m has been established using discrete components. The transmitter uses a low cost 'key - chain' laser as the source. The receiver is PIN diode based, with a JFET as the front -end amplifying device. In this thesis, the design and realiz ation of a low noise feedback receiver with particular attention to preamplifier stage is dealt with in detail. Circuit simulation of the preamplifier stage using Micro -cap is also included. Simulated results are also compared with actual measured paramete rs

For more details click here **back**

Title : *A Wide Band Mm-Wave Triplexer In Suspended Stripline*
Author(s) : *Singh Bhupinder*
Supervisor(s) : *SachidanandaM*
Roll No : *9910419*

Abstract:

For more details click here **back**

Title	***:***	***Design And Implementation Of IRDA Compatable Point To Point Optical Wireless Link For Indoor Applications***
Author(s)	***:***	***Bai A Swarna***
Supervisor(s)	***:***	***John Joseph***
Roll No	***:***	***9910404***

Abstract:

in recent years Wireless Infrared (IR) communication systems are being used widely to provide portable data communication at lower cost IrDA standards have emerged in order to meet the growing demand in this field. In this thesis an attempt has been made to design an IrDA compatible Indoor point-to-point experimental link with IR LED as a source and PIN photodiode as a detector. IrDA compatible encoder and decoder were designed and implemented in order to reduce the current requirements for driving the IR LED for various data rates. The IR link was tested with a PRBS generator for evaluating the system performance. Current-Intensity characteristic of the LED Source was measured. Sensitivity, Dynamic range and maximum data rate capability of the PIN photodiode based transimpedance amplifier were measured. The experimental link along with encoder and decoder was tested and the maximum range achieved was 30 cm at a data rate of 115.6 kb/s (1.2 Mb/s after encoding) with single IR LED as the source. The experimental link without encoder and decoder was interfaced to the RS-232 port of the PC and files were transferred from PC to PC for baud rates from 9.6 Kb/s to 57.6 Kb/s upto a distance of 10cm

For more details click here **back**

Title	:	*Analytical Modeling Of A FLBM-Based All Optical Packet Switch*
Author(s)	:	*Kushwaha Amit*
Supervisor(s)	:	*Bose Sanjay Kumar&Singh Yatindra Nath*
Roll No	:	*9910410*

Abstract:

In this thesis, the performance of an all-optical packet switch based on a multi-wavelength fiber loop memory is analyzed. The thesis develops an exact analytical model for the analysis of the switch and also suggests some approximations that may be used to examine the performance of large switches. The architecture and operation of the switch is based on the FLBM of the RACE-ATMOS project where individual wavelengths are used to store fixed length packets in a fiber-loop buffer. The architecture and mode of operation of this switch has been presented. The modeling of the switch is done for two conditions. In the first condition, reading and writing on a particular wavelength cannot be done in the same time slot. A switch of this type is referred to as a Type LSwitch. The other condition is one where a particular wavelength can be read from and written into in the same time slot. This switch is referred to as a Type U-Switch. Exact analytical models for both types of switches have been presented. These models have been used to determine the blocking performance of the switches and obtain their throughput and packet loss characteristics. The exact models have been used to study the performance of the switches under various loading conditions and for different values of the key design parameters of the switches. Numerical difficulties are encountered in using this approach for large switches. To tackle this problem, we subsequently develop an approximate queuing based approach, which may be used to study the performance of large sv^itches of both types. The results obtained by the exact method and the approximation models are compared to confinn that the approximations work well under typical loading conditions of the switch.tained solutions independent of initial population. This thesis has also outlined a methodology to obtain GA parameters which will produce consistent performance. YDES UNDER AEROBIC CONDITIONS : SCOPE AND MECHANISM

For more details click here **back**

Title **:** ***Compositional Verification Using Assume - Guarantee Approach***

Author(s) **:** ***Reddy P Prahallada***
Supervisor(s) **:** ***Roy Subir Kumar***
Roll No **:** ***9910461***

Abstract:

Formal verification based on Symbolic Model Checking has been successfully employed in the prefabrication verification of several System - On - Chip (SOC) designs. However, Symbolic Model Checking is beset with state and memory explosion problems which limits the size of designs that can be verified. SOC designs being inherently large, need to be verified using an approach based on "divide and conquer". Such an approach is, generally, taken intuitively by designers, based on the detailed knowledge of a design. In the present thesis, we verified the Cache Coherence Protocol of a split transaction bus of Pentium Pro (P6) for a case where it is reported in the literature that the symbolic Model Checking approach fails due to state explosion. We show ho w the above system can be verified using a Compositional Verification approach known as Assume -Guarantee approach. We illustrate how designers scan leverage their detailed knowledge of a design to partition it at the module level, and thereby, enable the A ssume - Guarantee approach to overcome intrinsic limitation of a formal verification tool to successfully verify large designs

For more details click here **back**

Title : *Controller Synthesis Of Asynchronous Digital Circuits*
Author(s) : *Bhanupratap B*
Supervisor(s) : *Roy Subir Kumar*
Roll No : *9910423*

Abstract:

problems related to technology migration, power consumption, critical path delay and clock distribution in large digital integrated circuits. Also, asynchronous circuits achie ve average case performance. Several methodologies exist for the design of asynchronous circuits, dependent on the models employed. In the present thesis we develop a systematic approach to controller implementation in the design of asynchronous digital sy stems based on the delay insensitive model using the non return to zero event driven signaling protocol. The controller is realized using a hierarchy of smaller controllers. This approach exploits the control information available in the control data flow graph derivable from the behavioral representation of a digital system. It also results in a simple interconnection network, which arises due to the sharing of functional and storage resources. We illustrate our approach by implementing several designs tak en from the literature. We also compare our approach with that present in the existing literature

For more details click here **back**

Title : *Spatial Domain Superresolution Reconstruction Of Images*

Author(s) : *Sisodia Kaushlendra Singh*
Supervisor(s) : *Venkatesh K S&Gupta Sumana*
Roll No : *9910440*

Abstract:

Superresolution (SR) reconstruction for a linear space variant point spread function (LSV PSF) is highly computationally intensive and generally ill conditioned. In this thesis we propose two algorithms for spatial domain reconstruction of SR images. The f irst algorithm includes recursive SR reconstruction of and image from several undersampled degraded frames, blurred by a space varying medium, with better reconstruction results than the existing method. The second algorithm includes a computationally effi cient method for separable PSF taking the fact that 2 - D shift matrix and 2 - D downsampling matrix are always separable and for getting a stable and unique solution of the ill -conditioned equations we use empirical regularized least square method

For more details click here **back**

Title : Automatic Jog Insertion In Layout Compaction
Author(s) : Gundavarapu Krishna Kumar
Supervisor(s) : RoySubir Kumar
Roll No : 9910443

Abstract:

Symbolic layout compaction plays a very important role in the physical design automation. Constraint-graph based compaction is one of the popular compaction procedures presents in the literature. Most approaches treat the wires as simply rectangular regions of variable length or width that can be moved rigidly from side to side during compaction. To reduce the layout area further, the rigid straight wire model can be replaced by allowing it to be bent. This is known as "jog insertion". Several approaches exist for introducing jog points in wires which will lead to reduction in layout area. In most of the jog insertion algorithms present in the literature, the basic layout primitive is restricted to a rectangle, and any mask polygon of an arbitrary shape in the Manhattan geometry is sliced into a number of rectangles. We propose an approach to overcome this limitation. Instead of using a rectangle as the primitive, we use a rectilinear polygon as a single basic entity. It has the advantage of minimizing the number of jog points, and therefore the number of nodes in the constraint graphs. This has the potential of resulting in lesser number of constraints in the linear programming (LP) formulation, used for solving the constraint graph. An algorithm for automatically and intelligently generating jog point in a layout is proposed in this thesis. Subsequent to finding the total jog points, the actual jog points are found, which lead to a minimization of the layout area. We propose a method using the constraint- graph approach to finally bend the wires at actual jog points. The implementation takes as input, a compacted mask layout description with rigid wire model, expressed in the industry standard Caltech Intermediate Format (CIF), along with a set of design rules specific to a fabrication technology and produces an output layout with lesser area due to jog insertion in wires

For more details click here **back**

Title : *Analysis Of Multicomponent Non-Stationary Models Using Wavelets*

Author(s) : *Prasad Keshava*
Supervisor(s) : *Sircar Pradip*
Roll No : *9910441*

Abstract:

The time - frequency representation of non - stationary signals tend to concentrate in separate regions in the time - frequency plane. Each region of energy concentration can be treated as a component of the signal. We model a non - stationary signal as a linear s uperposition of such components, where each component is characterized by its time -varying amplitude and frequency. A time - frequency selective approach is used for the estimation of the frequency and amplitude modulation laws of each component using wavele t transform. The components are first separated by the proposed algorithm. The instantaneous frequency is estimated by estimating the ridge as the set of local maxima of the transform square moduli and the time - varying amplitude is tracked as the amplitude variations on the ridge of the transform. The model is tested for synthetic and real life signals both in noiseless and noisy situations. The reconstruction accuracy of the model is also tested

For more details click here **back**

Title : ***Compressed Video Indexing And Retrieval System (CVIRS)***

Author(s) : ***Pandey Tej Pratap***

Supervisor(s) : ***Gupta Sumana***

Roll No : ***9910482***

Abstract:

One of the challenging problems faced in creating a multimedia database, is the organization of visual information. Since video requires a large amount of storage and processing, fast and efficient indexing, browsing, and retrieval of video has become a necessity. This can be achieved by analyzing the video directly in the compressed domain, thereby avoiding the overhead of decompressing the video into individual frames in the pixel domain. In this thesis a compressed video indexing and retrieval system (CV IRS) is developed. The video indexing tools support automatic segmentation of video, identification of key frames, and extraction of visual features. The visual features are used for efficient video retrieval and browsing. The proposed video indexing schem e uses the DC images of I and P - frames and macroblock information of P and b - frames, which are readily accessible from MPEG, with minimal decoding. Abrupt scene changes as well as special editing effects such as dissolves, fades etc. are accurately detecte d. The compressed domain approach proposed in this thesis is computationally less complex and uses less storage space as compared to the conventional methods. Unlike most of the existing methods, the proposed indexing scheme is robust to camera or/and obje ct motion and flashlight. Colour moments are stored as indices for key frames, and are used to retrieve the video frames efficiently. Some experimental results are shown to prove the validity of the proposed indexing and retrieval techniques

For more details click here **back**

Title	***:***	***Local Tomography Using Wavelet Transform And Extrema Extrapolation***
Author(s)	***:***	***Ravikanth M***
Supervisor(s)	***:***	***Gupta Sumana***
Roll No	***:***	***9910447***

Abstract:

In this thesis region of interest image reconstruction from projections using wavelet transform has been studied. In conventional filtered backprojection method, the exposure length of the object is usually increased due to the necessity of global projecti on data in non - local filters. Recently, algorithms have been developed using wavelets to essentially localize the Radon transform, so that the exposure length of the human body to harmful radiation can be decreased. In this work, a new technique is propose d using undecimated wavelet transform, for reconstruction of the inside and the outside of the region of interest (ROI). This technique eliminates unwanted information outside ROI as was present in the images reconstructed using earlier wavelet based algor ithms. We also develop a technique to reduce the exposure length using wavelet extrema extrapolation for the estimation of detail images. The proposed schemes are implemented using Shepp -Logan Phantom image as well as a real MRI image

For more details click here **back**

Title	***:***	***Joint Indexing And Watermarking Of Video Sequences In Compressed Domain***
Author(s)	***:***	***Bhardwaj Asheesh***
Supervisor(s)	***:***	***Gupta Sumana***
Roll No	***:***	***9910417***

Abstract:

The emerging techniques of content based indexing and retrieval of video signals and itsapplications for internet and MPEG-7 standards demand efficient approach for copyrightprotection of digital media watermarking is one such technique that provides copyrightprotection of digital video. In this thesis, a unique technique for Joint Indexing and Watermarking ofcompressed video bitstream is proposed. The method employs video segmentation ofcompressed bitstream followed by extraction of key frames. The features of the extractedkey frames are used both for watermarking as well as an index for retrieval. This reducesstorage space and reduces computational complexity to a great extent. The basic principle for embedding additive digital watermarks into compressedvideo is similar to spread spectrum communications. It consists of adding to a videosignal an encrypted, pseudo-noise signal that is invisible, statistically unobtrusive, androbust against manipulations. The proposed embedding technique takes into account thesensitivity of the Human Visual System (HVS) to luminance and colour components. Theseed used for generating the specific pseudo-noise signal is extracted from the first ordermoments of the three colour components (one luminance and two chrominance) of thekey frames. The watermark is generated by multiplying the Just Noticeable Difference(JND) to the pseudo-noise signal. The watermark generated is transformed using thediscrete cosine transform (DCT) and embedded into the video bitstream withoutincreasing the bit rate. The watermarks have been applied to all three colour componentsof a video signal. The watermarks can be retrieved from the decoded video without theknowledge of the original unwatermarked video.The proposed method is robust against common signal processing manipulations such aslowpass filtering, subsampling, collusion and cropping. The method is less complexcompared to the methods that decode the video bitstream for watermarking in pixeldomain followed by re-encoding

For more details click here **back**

Title	***:***	***Enhanced Fs-Aloha (E-Fs-Aloha) Algorithm For Contention Resolution In Wireless ATM Systems***
Author(s)	***:***	***Sood Deepak Kumar***
Supervisor(s)	***:***	***Sinha Vishwanath***
Roll No	***:***	***9910428***

Abstract:

In wireless network, the broadcast nature of the radio channel requires the introduction of a Medium Access Control (MAC) layer, in order to coordinate the access to the shred radio channel. A MAC protocol should not only avoid collision and distribute the available bandwidth in an efficient way, but should also support QoS provisioning. The delay experience on the contention period of the MAC frame has major impact on the delay performance of the MAC protocol, hence a delay efficient Contention Resolution Algorithm is required to satisfy the QoS contract. This thesis presents a Collision Resolution Algorithm, denoted as Enhanced FS -ALOHA (E - FS -ALOHA). This algorithm is used to inform the Base Station about the bandwidth needs of the Mobile Stati ons in a Wireless ATM network. E - FS - ALOHA is based on original FS - ALOHA algorithm, which groups the requests arrived at the mobile terminals during a frame length and serves these groups (Transmission Sets) on a FIFO basis using slotted ALOHA. The efficien cy of FS - ALOHA decreases with the total number of slots assigned for contention mechanism. In the proposed algorithm the overall performance (throughput and delay) of FS - ALOHA is further improved by serving two sets at a time instead of just one (as in FS - ALOHA) over the total contention period. Only when the number of available contention slots are less (i.e. of contention slots less than six) the maximum throughput achieved by E - FS - ALOHA is somewhat lower than the one attained by the FS - ALOHA. However th e delay performance of E - FS - ALOHA is always superior to FS - ALOHA. The complexity of E - FS - ALOHA is comparable to that of FS - ALOHA, but is requires no additional transmission bandwidth for its operation as compared to FS - ALOHA. The performance of E - FS - ALOHA is analyzed via simulation

For more details click here **back**

Title : ***Non Linear Frequency Warping In Speaker Normalization***

Author(s) : ***Vinay M K***

Supervisor(s) : ***Umesh Srinivasan***

Roll No : ***9910485***

Abstract:

In an effort to utilize the additional information available from the classical speech analysis studies regarding the nature of spectral scaling among speakers, a non - linear scaling function is proposed, for speaker normalization. The proposed non - linear s caling function is independent of the phoneme class and is completely derived from vowel formant database. This non - linear scaling function has been analysed using various methods like formant data analysis, spectral alignments and HMM - based recognizers. U sing separability measures like F - ratio and residual variance, the proposed method is found to be superior to linear scaling for formant data analysis. A warping function and hence a non - linear scale invariant transformation is derived from this non - linear scaling function, to be incorporated into a HMM - based recognizer. Using recognition accuracy as a performance measure the proposed transformation is compared with other similar schemes. Our results suggest that further studies are necessary to enable effe ctive use of non - linear scaling functions on HMM - based recognizers.

For more details click here **back**

Title	***:***	***Study Of 3gpp WCDMA (FDD) Downlink For Software Configurable Radio Base Station Systems***
Author(s)	***:***	***Bellam Sasi Kumar***
Supervisor(s)	***:***	***Sinha Vishwanath***
Roll No	***:***	***9910422***

Abstract:

generation cellular base stations use dedicated hardware to realize physical channels. They employ a bank of narrow band transceivers one for each channel. The cost/compl exity of these base stations grows linearly with the number of supported channels. Also, seamless global roaming in multi - standard environments is not supported by the present generation system. In contrast, software radio/virtual radio approach provides r econfigurability of the system. In this approach all physical channels, are realized using software modules that run on a processing platform with wideband ADC at front end. The ADC digitizes the whole service RF band for subsequent software processing. In strict sense software radio uses Digital Signal Processors (DSPs) while virtual radios uses general - purpose processors for software processing of digital bit stream from the ADC. The advantages of software only approach are numerous such as support of glo bal roaming in multi - standard environments, ease in upgradation as it eliminates the need to replace the dedicated base station hardware etc. However, the difficulty in the software - approach realization of a cellular system is the requirement of high dynam ic range wideband ADCs as well as heavy processing power requirements for software processing of bit streams. The goal of next generation mobile communication system popularly called as Third Generation (3G) Cellular Systems, is to seamlessly provide a wid e variety of communication services such as high speed data, video and multimedia traffic as well as voice traffic. One of the most promising air interface that is accepted worldwide that meet 3G requirements is the Wideband Code Division Multiple Access (WCDMA). In the present work we have focused on processing power requirement part of the software - only approach and have studied the feasibility of realization of 3G WCDMA base station systems in software. We have assumed virtual radio environment for our w ork. Using C language we have realized all downlink physical channels for FDD mode of 3GPP WCDMA base station system according to physical layer specifications of the 3GPP group. Each downlink physical channel is realized by implementing all its physical l ayer operations such as CRC coding, channel coding, rate matching interleaving, spreading and scrambling in software. By executing all the above operations for each downlink physical channel on a general purpose processor (virtual radio approach) the compu tational power required to realize each downlink physical channel has been estimated and expressed in terms of %CPU metric and in terms of SPEC ratings. As the computational power expressed in%CPU metric depends on the processor used, SPEC ratings are used to express the computational power in a processor independent way. Three base station systems each with different downlink channels are assumed and computational power required to realized the whole downlink of each system has been evaluated. From the com putational requirements of each of the assumed base stations, a figure of computational power requirement for downlink in practical real time base stations has been estimated. From the results obtained in our work, we ob serve that the virtual radio approa ch is quite attractive but the realization cannot be supported by the computational power of present day processors

For more details click here **back**

Title **:** ***Estimation Of Motion And Depth From Smeared Images***

Author(s) **:** ***Bajpai Rajiv Kumar***

Supervisor(s) **:** ***Venkatesh K S& Gupta Sumana***

Roll No **:** ***9910468***

Abstract:

A method for estimating velocity from two successive frames of motion smeared images is described. The problem is posed as a system identification problem. The underlying phenomenon of motion smearing is modeled as a linear system with an appropriate trans fer function. An algorithm for estimating the transfer function is derived. The motion vector is estimated from the support of the corresponding point spread function. Further, a new method for estimating depth and motion simultaneously is presented. The m ethod uses the defocus and the motion - smear information present in the image frames. Both the methods are tested on simulated images

For more details click here **back**

Title	***:***	***Performance Analysis Of 2d-Rake Receiver In Low Processing Gain DS-CDMA Systems***
Author(s)	***:***	***Pradeep Kumar Sah***
Supervisor(s)	***:***	***Chaturvedi Ajit Kumar***
Roll No	***:***	***9910464***

Abstract:

In this thesis performance analysis of a 2D - RAKE receiver for low processing gain asynchronous DS - CDMA system with random binary sequence has been done. Since the processing gain is low, we have not assumed that the multipath interference (MPI) is Gaussian . Bit Error Rate evaluation indicates that 2D - RAKE receiver provides significant improvement over conventional RAKE receiver. As expected this improvement is affected by correlated fading among antennas of 2D - RAKE receiver. Results show that as correlation among received signals increases due to decrease in separation between antennas, system performance degrades. But this degradation is not significant if separation between antennas is greater than or equal to half of the carrier wavelength. Performance ga in of the system depends on the number of antennas and number of fingers in the 2D - RAKE receiver. We have found that if the number of users is large then effect of MPI is negligible. In this case, the Gaussian assumption for MPI can be taken

For more details click here **back**

Title	***:***	***Heuristic Converter Placement Algorithm And Study Of Its Effects On Sparse WDM Networks***
Author(s)	***:***	***Popat Bhoomika***
Supervisor(s)	***:***	***Bose Sanjay Kumar& Singh Yatindra Nath***
Roll No	***:***	***9910424***

Abstract:

Wavelength conversion plays an important role in enhancing fiber utilization and offers modes reduction in blocking probability by relaxing wavelength continuity constraint. However, introduction of wavelength converters in optical cross - connects (OXC) of Wavelength Division Multiplexed (WDM) networks increases the switch complexity and cost of the network. Thus, to achieve a tradeoff between cost, complexity and performance improvement offered by wavelength converters, sparse conversion networks are consid ered. In a sparse network, few of the nodes in network have full conversion capability. Finding the nodes in the network that should be equipped with full conversion capability for optimal performance is a NP - complete problem for a general network. A simpl e sub - optimal heuristic approach to this problem has been suggested in this thesis. In Wide Area Networks (WAN), some of the nodes are prone to heavier traffic and carry longer lightpaths as compared to rest of the nodes. It is intuitive to place wavelengt h converters at these nodes to reduce the blocking probability of the network. It is observed that few nodes as found by heuristic algorithm equipped with conversion capability, provides comparable improvement in blocking performance as a fully convertible networks. Conversion gain in terms of reduction blocking probability offered by sparse conversion networks, using heuristic placement algorithm is also studied for various routing schemes. Extensive simulation study has been carried out for NSFNET and ARP A2 networks with an objective to study effect of heuristic placement of sparse conversion networks. Converter utilization as found from simulation, show heavy usage of converters at the nodes selected by heuristic placement algorithm for sparse networks us ing metric based routing scheme. Reducing the number of converters at nodes selected by the proposed algorithm is also studied under metric based routing sc

For more details click here **back**

Title	***:***	***Simulation Studies Of OFDM Based Multicarrier CDMA Systems***
Author(s)	***:***	***Srungaram K S Venugopal***
Supervisor(s)	***:***	***Chatterjee P K***
Roll No	***:***	***9910445***

Abstract:

The recent trends in mobile communications is to provide higher data rate applications such as multimedia services and Internet access in addition to voice services. Most of these services are asymmetric in nature and demand for higher data rates from base station to mobile terminal (down link) than mobile terminal to base station (up link). Orthogonal frequency division multiplexing (OFDM) based multicarrier code division multiple access (CDMA) systems appear to be a promising solution for these applicatio ns. In this work a base station to mobile terminal link with OFDM based multicarrier CDMA is considered. The transmission in this scenario is synchronous and to support higher data rates multilevel modulation scheme, quadrature amplitude modulation (QAM), is used. QAM requires less bandwidth to support higher data rates than binary modulation but it requires more power to achieve the same performance. Since the down link transmission is under consideration such power requirements can be met at base station. The performance of multicarrier CDMA system in the down link is studied with QAM as the modulation scheme. The multicarrier CDMA system considered here is based on orthogonal Walsh sequences. The performance of QAM is studied starting from a simple additi ve white gaussian noise (AWGN) channel. Then the performance in the Rayeigh fading channel which is a more realistic model in mobile communication environment is studied with different detection strategies at the receiver. The effect of Rayleigh fading cha nnel is that it requires a large signal to noise ratio increment than that of simple AWGN channel. In multicarrier CDMA system to achieve a symbol error rate of 10 - 3 , 16 - ary QAM requires signal to noise ratio of 11.7 dB in simple AWGN channel and 31.6 dB i n Rayleigh fading channel with channel inversion technique. In Rayleigh fading channel with a diversity order of three, symbol maximal ratio combining requires 16.5dB and chip maximal ratio combining requires 15.5dB of signal to noise ratio, respectively a chieve the same symbol rate of 10 - 3 .

For more details click here **back**

Title : Modified Algorithms For 3g Security
Author(s) : Gollapudi Sreelakshmi
Supervisor(s) : Sinha Vishwanath
Roll No : 9910431

Abstract:

wireless communication system. The radio interface between the terminal equipment and the serving network represents a significant vulnerable point of attack. The thr eat associated with attacks on the radio interface are Unauthorized Access to Data, Threats to Integrity, Denial of Service Attacks, and Denial of Service by Masquerading as Communications Participant. Third Generation Wireless Communication System (3GPP) are targeted to provide a wide variety of services ranging from AMR (Adaptive Multi Rate - 4.75 Kbps to 12.2Kbps) speech to Primary EI data rate (2.048Mbps). In 3G wireless communications, users are authenticated based on USIM card (User Services Identific ation Module) in contrast to SIM (subscriber Identification Module) card in GSM/IS95 systems. In 3G, authentication and key agreement procedures prevent unauthorized users accessing the resources of serving network and home network. Authentication and key agreement requires MACs (Message Authentication Codes) to authenticate user to network and vice versa. Authentication and key agreement algorithm also requires key generation for generating the session keys, cipher key and integrity key. We study algorith ms that provide security especially in the 3G systems, with the objective of devising still robust algorithms. We consider various attacks, which compromise the communication security. In this thesis HMAC (Hash based MAC) version of modular arithmetic hash function MASH has been proposed as new key generator. HMAC is an efficient way of constructing MAC from unkeyed hash function. Modified form of CBC - MAC (Cipher Block Chaining MAC) and another new block cipher based MACs are proposed for MAC functions in a uthentication and key generating algorithm. Mathematical analysis of proposed algorithms has been carried out to show that the proposed algorithms satisfy 3G requirements. We show that the proposed algorithms meet ideal MACs and standardized Key Generators ’ robustness to the attacks of intrudes. Through statistical analysis we show that the output sequences randomness properties of the proposed algorithms closely match the standardized algorithm output sequences randomness properties. The proposed MAC algor ithm1 has the advantage of less complexity in terms of processing the information compared to already existing CBC - MAC algorithm. MAC algorithm2 is a still more efficient way of using CBC - MAC for meeting 3G F2 requirements. Proposed Key Generator is an exa mple of using modular arithmetic and HMAC strategy together for generating session keys.

For more details click here **back**

Title	***:***	***Path-Metric Based Routing For Dynamic Operation Of WDM Networks With Varying Conversion Capabilities***
Author(s)	***:***	***Raju A N V B***
Supervisor(s)	***:***	***SinghYatindra Nath& Bose Sanjay Kumar***
Roll No	***:***	***9910402***

Abstract:

Wavelength Division Multiplexed (WDM) all - optical networks, with several optical wavelengths multiplexed on individual fibers, are expected to provide the communications resources for both long and short - haul networks in the near future. This thesis propos es path - metric based routing algorithm for dynamically operating a Wavelength Division Multiplexed (WDM) network with limited conversion capability. The optical cross connect switches (OXC) at the network nodes are assumed to gave limited number of convert ers which may be used in a share - per - link or shared - per - node architecture. Typical operation of this kind of network assumes a single fixed path (i.e. shortest - path using Dijkstra's Algorithm) between source and destination and limits itself to choosing th e wavelengths to be used over the various links. We consider a more general approach where multiple candidate paths between the source and the destination are quickly examined using a path - metric based strategy. Our proposed algorithm uses this metric base d approach to find the best choice regarding which wavelengths should be used in the component links and the nodes at which wavelengths are to be converted, if any. The performance of the proposed algorithm is studied using simulations on the NSFNET and AR PANET network

For more details click here **back**

Title	***:***	***Resource Allocation For Combined Voice And Data Users In Cellular DS-CDMA System***
Author(s)	***:***	***Kumar Satyendra***
Supervisor(s)	***:***	***Chaturvedi Ajit Kumar***
Roll No	***:***	***9910474***

Abstract:

We consider a packet data DS - CDMA system which supports multiple services. The services are partitioned into different traffic classes according to transmission rate and quality of service. An analytical method of allocating resources viz. power and proces sing gain to different classes of users in the presence of other cell interference and imperfect power control for both uplink and downlink is presented. We consider two models for data users: random and continuous. We maximize the throughput of data users by finding the optimal processing gain of data users for a given value of processing gain of voice users. The quality of service measures considered are: average delay for data traffic and bit error rate for voice traffic

For more details click here **back**

Title : ***Pulse Shaping For Multicarrier Modulation In Doubly Dispersive Channels***

Author(s) : ***Pandey Anil***

Supervisor(s) : ***Chaturvedi Ajit Kumar***

Roll No : ***9910411***

Abstract:

Single carrier systems use equalizers to remove channel impairments. The increase of data rate increases equalizer complexity making its implementation difficult. The idea of multicarrier modulation is to transmit high rate data over many carriers by divid ing it into several low rate data streams and hence making equalizer design potentially simpler. But placing many carriers in same available bandwidth gives rise to Inter Carrier Interference (ICI). To get ICI free transmission at least in ideal channel, c arriers must be orthogonal to each other. Pulse shape used to represent a symbol, plays an important role in reducing ICI. But pulse shaping has a limitation that the pulse decreasing ICI makes it sensitive towards ISI. Though ICI cab also be decreased by increasing carrier spacing, but it will decrease the spectral efficiency of system. Hence pulse shaping can give a compromise between ISI, ICI and spectral efficiency, in order to minimize total interference. Delay dispersion of channel gives rise to ISI a nd doppler dispersion to ICI. Hence pulse design should also depend upon the channel characteristics in which it has to be used. In this thesis pulse shaping issues have been considered and orthogonal as well as non -orthogonal pulses have been compared for doubly dispersive channels

For more details click here **back**

Title	:	*Downlink Performance Evaluation Of DS-CDMA System Over Nakagami-M Fading Channel*
Author(s)	:	*Patel Prabhat*
Supervisor(s)	:	*Chaturvedi Ajit Kumar*
Roll No	:	*9910463*

Abstract:

IS - 95 is the only CDMA based second generation standard for cellular communication. Its performance has been evaluated over Rayleigh fading channel by many investigators. However, Nakagami - m channel model is considered to be more appropriate for frequency selective fading channels. It includes the Rayleigh fading channel and one sided Gaussian as special cases. In this thesis the BER performance of forward link (base station to mobile station) of IS - 95 standard has been evaluated. The multipath channel mode l assumes independent paths with Nakagami - m fading statistics. RAKE receiver has been used to evaluate the performance under various multipath fading conditions. The results indicate that for m<1, the performance is worse when compared to the performance w ith Reyleigh fading channel model, whereas it gets better for m>1. Also, more than 20 users can access the channel (assuming 64 chips Walsh code) simultaneously and can achieve uncoded BER of 0.01 with an average SNR of around 10dB

For more details click here **back**

Title : *Application Of Multiuser Detection To Is-95 Reverse Link*

Author(s) : *Kambalyal Vishwanath S*

Supervisor(s) : *Chaturvedi Ajit Kumar*

Roll No : *9910486*

Abstract:

In Direct - Sequence Code division Multiple Access (DS - CDMA) systems, conventional detection uses the matched filter and the desired user's spreading sequence. It does not exploit the structure of Multiple Access Interference (MAI). This results in sub - optim al performance. Iterative techniques like Serial and Partial Parallel Interference Cancellation in Multiuser Detection (MUD) have been widely studied for short spreading sequences. However, recently interest has been generated in long spreading sequences. In this thesis simulation studied have been done for different iterative techniques for MUD in the existing long code based second generation (2G) IS - 95 mobile communication standard. The channel environments considered are MAI, Gaussian and Rayleigh. Two new algorithms with better performance have been proposed. Effect of near - far problem on MUD performance has also been studied

For more details click here **back**

Title	***:***	***Development Of An IP Core Network Model For Performance Analysis Of Third Generation Radio Access Networks***
Author(s)	***:***	***Baig Mirza Shahrukh***
Supervisor(s)	***:***	***Sinha Vishwanath***
Roll No	***:***	***9910450***

Abstract:

Third - generation (3G) mobile communication systems like General Packet Radio server (GPRS) Universal Mobile Telecommunication Standard (UMTS) new standards have to be integrate d into the existing mobile radio networks. The driving force for this development is the predicted user demand for mobile data services that offer mobile Multimedia access and mobile Internet access. Since radio resources are scarce, Quality of Service (Qo S) issues become very important for scalable use of these resources. Moreover as we move from circuit - switched to packet - switched services many changes have to be brought about in the existing networks to fulfill ever growing user demands like voice, vid eo, time sensitive financial transactions. still images, large data files and so on. For performance analysis of 3G mobile data services both radio network and the core network have to be modeled to regard end - to - end Quality of Service behavior. Thus in t his thesis a router model is developed which emulates the scheduling functions of an IP router as part of 3G Core Network based on Third Generation Partnership Project (3GPP) standards. Further an IP core network model (based on DiffServ) is set up which is then integrated into the ComNets GPRS simulator GPRSim. On the basis of simulations, this integration is evaluated for differentiated service performance. Finally DiffServ capable IP is compared with the present IP which is best effort

For more details click here **back**

Title : ***Speech Enhancement Using Kalman Filter With Spectral Constraints***

Author(s) : ***Shrivastava Sudeep***

Supervisor(s) : ***Chatterjee P K***

Roll No : ***9820408***

Abstract:

Speech signals are often degraded by additive noise. The degradation of speech by background noise can adversely affect the performance of a speech processing system. In this work, improved form of iterative speech enhancement id formulated. Kalman filter with spectral constraints is used iteratively for filtering speech contaminated by additive white or coloured noise. The results indicate significant improvement in SNR and audible improvement in output speech quality over previous work done using kalman f ilter for both white and coloured noise. Also in this thesis, a modified algorithm has been formulated for speech signal degraded by additive crosstalk noise or babble over single channel communication. The efficacy of the algorithms have been established by objective distortion measure and subjective listening tests

For more details click here **back**

Title : ***A Novel Representation Of Color Signal For Compression Applications***

Author(s) : ***Ramana N V***

Supervisor(s) : ***Gupta Sumana***

Roll No : ***9810432***

Abstract:

The new representation of colour signals for compression applications proposed in this thesis, is aimed at reducing the large perceptual redundancy present in the colour representation. The method employed combines the two chrominance signals U and V into a single signal. This is achieved by the spiral mapping of U – V signals. The statistical properties such as the entropy, variance and correlation of the new signal is calculated for several color images. The bandwidth and colour approximation noise ratio (CSANR) also derived for the new signal. To reduce the noise problems, approximated single signal is squared. Simulation experiments are performed on several color images to establish the validity of the spiral approximation with as few encirclements of th e spiral has possible. To improve the color quality of reproduced images, the spiral is made to vary along Y - the luminance axis, according to the varying nature of color gamut. For the propose of data transmission the new color signal has been encoded with embedded zero tree coding algorithm, and a bit rate of 2 to 3bits/pixel is found to produce acceptable quality images.

For more details click here **back**

Title	***:***	***Automated Visual Inspection Of Steel Surface, Texture Segmentation And Development Of A Perceptual Similarity Measure***
Author(s)	***:***	***Guha Prithwijit***
Supervisor(s)	***:***	***Gupta Sumana& Mukerjee Amitabha***
Roll No	***:***	***9910465***

Abstract:

In this thesis work we describe the prototype system developed for Real Time Visual Inspection of Cold Rolled Steel Surface Defects. The proposed system aims at detecting four classes of surface defects, viz. Anneal Colour, Black Patch, Hole and Indentation Mark. The prototype system hosts a simulated conveyor drive for keeping steel sheets m motion along with an imaging setup consisting of a well designed illumination system and an interlacing camera interfaced with Matrox Meteor II image acquisition card operated through a Pentium Class Processor. Content based image retrieval techniques have been used for detection and classification of surface defects. The image blocks are submitted as queries, which are processed for defect identification through Artificial Neural Network based Colour Histogram Feature Classification, Surface Modeling and Image Thresholding. The thesis also discusses algorithms for textural feature extraction and classification applied to supervised segmentation of multi-textured images, which could be extended to identify defects that are characterized by textures. More so, we propose a new measure of visual similanty developed on a perceptual framework. The new measure computes the indices of similanty (dissimilarity) between the query and the image database, thereby providing psycho-visually viable image retneval results. We also discuss the possible application of the new measure to the problem of defect classification as an alternative procedure of content based image retneval. Finally, the thesis discusses the possible future extensions to the prototype system along with suggestions to develop the high-speed industrial inspection system based on parallel imaging hardware.

For more details click here **back**

Title : Color Quantization For Video Sequences
Author(s) : Gnanaraj D Godwin
Supervisor(s) : Venkatesh K S
Roll No : 9910427

Abstract:

Many display devices nowadays still allow a limited number of colors, called color palette, to be displayed simultaneously. Besides, images and videos in most World Wide Web databases are in compressed formats (JPEG, MPEG). Therefore, it becomes important an issue to retrieve a suitable color palette from compressed domain in order to have fast and faithful color reproduction for these devices. In this paper, color palette design methods for compressed images and videos are presented. The proposed approach uses the reduced i.e. DC image, rather than the whole, image for color palette design to avoid computation involved in image or video decompression. In this approach we use a combination of sequential scalar Quantization and uniform color space representation to accomplish the color palette design. The color palette is refined over subsequent frames for better color reproduction of images. Experimental results show that output image quality of proposed methods is acceptable for human eyes

For more details click here **back**

Title **:** ***Color Image Segmetation Using Watershed Algorithm***
Author(s) **:** ***Jain Prabhat***
Supervisor(s) **:** ***GuptaSumana***
Roll No **:** ***9910462***

Abstract:

Watershed based image segmentation has gained much popularity in the field of biomedicine and computer vision where large images are not uncommon. In this thesis a fast and flexible algorithm for computing watersheds in digital color images is introduced. The present algorithm is based on the immersion process analogy, in which the flooding of the water in the picture is efficiently simulated using a queue of pixels. The color information is effectively used using homogeneity criterion and it is shown that use of color information gives far better results in almost same time as that of given by simple watershed algorithm. The strongest point of the present algorithm is that it is faster than any other existing watershed algorithm. Apart from that the accuracy of the present algorithm is far better than any other algorithm available. in

For more details click here **back**

Title : Priority-Based Scheduling Policies For Bluetooth
Author(s) : Babu D Raveendra
Supervisor(s) : Sinha Vishwanath
Roll No : 9910469

Abstract:

Bluetooth is a wireless adhoc network concept primarily intended to eliminate the cables between computers, cell phones, PDAs etc. the Bluetooth radio nodes form adhoc networks called piconets. A Bluetooth unit can participate in more than one piconet at any time but it can be a master in only one piconet. A unit that participates in multiple piconets can serve as a bridge thus allowing the allowing the piconets to form a large network. A set of piconets that are all interconnected by such bridging units is referred to as a sactternet networks. In any communication system, it is important to support various traffic with QoS (Quality-of-Service) guarantees. Broadly, diverse traffic may be categorized as real-time traffic and non-real-time traffic. Bluetooth supports both real-time and non-real-time communication services. A non-real-time communication service in Bluetooth is considered. Depending on its distinct characteristics and QoS requirements, the non-real-time traffic can be divided into two classes: a) class1: delay-tolerant traffic like paging and email; and b) class2: delay-sensitive traffic like FTP and remote log-in. the main distinguishing factor between these classes is how delay sensitive the traffic is. The purpose of present work is to support different classes of service (class1 and class2) in Bluetooth through priority and scheduling mechanisms. In our proposed methods, class2 traffic is given priority over class1. The two important parameters that have been considered are minimizing end-to-end packet delivery delay and providing consistent data throughput and capacity. We examine in detail performance of non-real-time communication service in Bluetooth

For more details click here **back**

Title : *Comparison Of Performance Of Artificial Neural Network On Typical Benchmark Problems Using MATLAB Tools Vis-A-Vis Codes Written In Java*

Author(s) : *Kumar Sushil*
Supervisor(s) : *Kalra Prem Kumar*
Roll No : *9910481*

Abstract:

An attempt has been made in this project to find optimum neural network configuration, using MATLAB Toolbox, for some of the benchmark problems. These problems are considered difficult to solve, using standard ANN techniques. Beside these problems some com plicated functions have also been considered and an attempt has been made to solve them. All the problems considered in this work are typical in the sense that they capture the extremities of most of the parameters. Problems considered fall in the category of Classification and function Approximation. Codes developed in JAVA were used to solve the sane problems. The results thus obtained were used to compare to that obtained by using MATLAB Toolbox. The codes developed using JAVA have undergone refinement may be used for modeling of Neural Networks for real life problems

For more details click here **back**

Title	***:***	***Modeling And Simulation Of Two-Electrode And Three-Electrode Plasma Cells For A Plasma Display Panel (PDP)***
Author(s)	***:***	***Pandey Kamlesh Kumar***
Supervisor(s)	***:***	***Das Shyama Prasad***
Roll No	***:***	***9910438***

Abstract:

In this work an electrical equivalent circuit model for a two - electrode as well as for a three - electrode ac plasma display panel (PDP) cell is developed. The model qualitatively explains the gas discharge phenomena such as time - delay to breakd own, wall voltage buildup, collapse of gas gap voltage, and nature of discharge current during discharge activity. Using this model various important electrical characteristics of a PDP cell such as, voltage transfer curve, discharge current, displacement current, wall voltage variation with respect to time, and gas gap voltage variation with respect to time are obtained and compared with the standard results. From the transfer curve, various ac PDP cell - operating parameters such as, sustain margins, erase pulse limits, and write pulse limits are obtained and matched satisfactorily with the available results of the fluid models

For more details click here **back**

Title	***:***	***Voltage Stability Enhancement Using Facts Controllers Under Contingencies***
Author(s)	***:***	***Naidu B Jagannadha***
Supervisor(s)	***:***	***Srivastava S C***
Roll No	***:***	***9910433***

Abstract:

The voltage instability occurs in power system networks mainly due to the reactive power shortage or difficulty in transmitting the required reactive power to the loads. A power sys tem becomes more vulnerable to voltage instability due to the outage (contingency) of any branch of its transmission network. Hence, it has become important to consider the voltage stability criterion also in system security assessment. For secure operatio n of power system, it is necessary to identify the contingencies causing voltage instability (critical contingencies) and plan for the on line remedial actions in order to avert voltage collapse in the system. The present work has made an attempt in this d irection. For ranking contingencies considering voltage stability criterion, a new scalar index called as Reactive power Loss Index (RPLI) has been proposed. With the help of sensitivity of the new scalar index optimal location of Flexible AC Transmission Systems (FACTS) controlled Series Compensator (TCSC) and Static Var compensator (SVC) have been determined. In addition, with proper combination of series & shunt devices sensitivity factors, optimal location of Unified Power Flow Controller (UPFC) has bee n suggested in the network. A method for optimal adjustment of UPFC parameters ahs been suggested for alleviating the voltage instability under contingency conditions. The proposed methods have been tested on two IEEE test systems.

For more details click here **back**

Title	:	*Analysis And Modelling Of Benchmark Problems With Multi-Layered Feed-Forward Neural Networks*
Author(s)	:	*Sreeram A*
Supervisor(s)	:	*Kalra Prem Kumar*
Roll No	:	*9910403*

Abstract:

process modeling over the past one decade. Among the different neural network architectures, the feed forward neural networks are most widely used. From time to time, a lo t of benchmark problems have been developed to analyse the performance of mulit-layered feed- forward neural networks. These problems are typical of the problems used by researchers to test various performance characteristics of MLFF networks and to verify theoretical results through simulation. In the present thesis work, an attempt has been made to analyse these benchmark problems as well as a few more typical model problems in classification and function approximation areas using multi-layered feed-forwar d neural networks under back- propagation paradigm to check how typical these problems are to be used as standard benchmarks. These problems have been solved with network models developed using MATLAB neural network toolbox. These models were developed for the benchmarking and evaluation of training algorithms developed on JAVA platform, against MATLAB, being a standard package, as a part of the ongoing BARC project. Effects have been directed toward solving maximum number of benchmarks and typical complicat ed problems to acceptable accuracy levels so that these become standard neural networks models to evaluate the performance of the JAVA algorithms. The problems considered cover most of the aspects of neural network theory

For more details click here **back**

Title : *Allocation Of Congestion Management And Voltage Regulation Cost Using Power Tracing Approach*

Author(s) : *Kumar Ajay*

Supervisor(s) : *Srivastava S C&Pai Mangalore Anantha*

Roll No : *9910406*

Abstract:

he main objective of these changes is to allow for competition among various market players, to offer a low price, higher quality and more secured product. These chang es call for many new practices to the power system operation and are also accompanied by variety of problems. Under a competitive environment, generation is not centrally dispatched, but rather, it is based primarily on the transactions agreed to in the op en market. In the market situation, the difficulty lies in ensuring the negotiated transactions, particularly under congestion and also maintaining system bus voltages within limit. The task is generally carried out by an independent system operator (ISO), through purchase of additional real and reactive powers from ancillary sources in the system. An optimal power flow based method has been used in this work to compute the additional generation required from ancillary sources to remove congestion without c urtailment of bilateral transactions. Real power tracing has been utilized for equitable allocation of cost of the congestion management among various market participants. Voltage profile management has been achieved through additional reactive power purch ased from ancillary sources in the form of shunt compensatory devices. Allocation of cost of the voltage regulation has also been suggested by using reactive power tracing. Studies have been conducted on modified IEEE - 14 bus and IEEE - 30 bus systems. The pr oposed method shows quite fairness in allocation of cost of congestion and voltage regulation to the market participants.

For more details click here **back**

Title	***:***	***Analysis And Simulation Of Multilevel Inverters For Static Compensators***
Author(s)	***:***	***RaoV V N K Someswara Koduri***
Supervisor(s)	***:***	***Joshi Avinash***
Roll No	***:***	***9910484***

Abstract:

Power electronic equipment's convert power from to other, as required by the consumer, with ease of control and high efficiency. These power electronic equipment have inherent non - linear characteristics, introduce harmonics into the source. In this Thesis several voltage source inverter structures are made to operate as current source inverters to compensate the load. The load currents are sensed and reference currents for the compensator are generated, which would make the source current sinusoidal and mai ntain the unity power factor. Using various current control techniques the compensator current is made to follow the reference currents. Thus the source only provides real power while the reactive power and harmonics are provided by the compensator. In the end of the thesis, a new multilevel inverter structure that can compensate much better than a conventional 2 - level inverter when the loads contain only ac components is proposed.

For more details click here **back**

Title : *An Approach To Frequency Based Generation Cost Computation*

Author(s) : *Rao M Krishna*
Supervisor(s) : *Kalra Prem Kumar*
Roll No : *9910444*

Abstract:

Many countries in the world have opened their power markets to allow the competition between the power producers. The affect of the load changes on the operating frequency and real power output of the generator have been studied in the present work. If the frequency goes out of the limits the generator may loose synchronism. The frequency of the system should be maintained with in acceptable limits. In an interconnected power system, change in load of one control area will also affect the frequency and gene ration of the generators in other control areas. The variation in generation cost because of these deviations in frequency and real power output of the generator have been studied for a single control area case. The excessive generation cost because of the load change in this control area can be charged to that particular user. The powerful Newton - Raphson method has been used for solving the load flow problem generation has been optimized using optimal power flow. Load frequency control has been used to cal culate the frequency deviations.

For more details click here **back**

Title	***:***	***Generation Pricing For A Single Area Power System Using Modified Second Order Newton-Raphson Techniques***
Author(s)	***:***	***Hari Chakrapani K***
Supervisor(s)	***:***	***Kalra Prem Kumar***
Roll No	***:***	***9910436***

Abstract:

The Newton - Raphson method is a powerful tool to solve the non - linear equations or simultaneous equations. It is popular due to its fast convergence properties. The modifications suggested in literature over standard NR is to accommodate ill conditioning an d improve the speed of convergence. Large number of variations of NR suggested in literature are only for single non - linear equation. However, it has been observed that it is not possible to extend these methods to a set of non - linear equations in straight forward fashion. This thesis work presents various modifications of NR for solving set of non - linear equations. Sudden change in load in power system will cause change in frequency as well as real power demand. Cost of generation is made as a function of f requency and real power demand. Present thesis work integrates both these changes and provides a mathematical framework for calculation of generation pricing.

For more details click here **back**

Title	***:***	***Determination Of The Available Transfer Capability In A Deregulated Power System***
Author(s)	***:***	***Srivastava Anshuman***
Supervisor(s)	***:***	***Srivastava S C***
Roll No	***:***	***9910413***

Abstract:

Power industries in many parts of the world have been deregulated to introduce competition among the market participants and bring several competitive opportunities. A fair competition needs open access and non-discriminatory operation of the transmission network. Open access to the transmission system places an emphasis on the intensive use of the interconnected network reliably, which requires knowledge of the network capability. Available transfer capability (atc) is a measure of the remaining power transfer capability of the transmission network for further transactions. This work gives an approach to calculate atc of the transmission path. Atc determination models are developed using the static and dynamic criteria. Under static criteria, line thermal limit, bus voltage limit, generator real and reactive power limit and voltage stability limits are considered. The Newton raphson load flow method and the continuation power flow method are used as tools for static atc calculation. The static atc determination model is tested on two real systems, the Icelandic 220kv system and the upseb 400kv system of India. Under dynamic criterion, only steady state stability limit has been considered. The dynamic atc determination model is tested for a single machine infinite bus (smib) system. The developed models provide a step-by-step procedure for atc calculation. It calculates the transfer capability for each of the static and dynamic criteria and indicates the limiting condition that restricts the value of atc

For more details click here **back**

Title : *An LCLC Resonant Dc-To-Dc Converter With PWM Control-Analysis, Simulation And Implementation*

Author(s) : *Singh Kamal Jeet*

Supervisor(s) : *Doradla S R& MutschlerPeter*

Roll No : *9910437*

Abstract:

Among various possible four element resonant dc-to-dc converters, the topology which takes the parasitic elements of the output high frequency transformer and output diode bridge is presented. High frequency resonant dc-dc converter finds wide spread applications in power supplies due to their small size and light weight with fast transient response. Although this topology is referred in the literature very briefly as a four-element circuit, no detailed study of such a topology is reported in the literature. The steady state characteristics using simple ac circuit analysis are presented. The four-element resonant converter is shown to exhibit load-independent operation at two switching frequencies, one below and the other above the resonant frequency. These characteristics are verified using a simulation called PECSIM (Power Electronics Circuit Simulation). The dc-to-dc converter is designed for a maximum power output of 500 W (100 V, 5 A) and at a switching frequency of 100 kHz which is above the resonant frequency. The switching frequency is held constant and output voltage is varied by pulse width modulation (PWM). The results obtained from the circuit implementation agree well with the simulation results

For more details click here **back**

Title : ***Investigation Of The Effect Of Laser On The Breakdown Strength Of Atmospheric Air With Lighining Impulse Voltage***

Author(s) : ***Singh Sudhir Kumar***

Supervisor(s) : ***Arora Ravindra***

Roll No : ***9910480***

Abstract:

Laboratory investigations were carried out to study the effect of laser radiation on the breakdown strength of the air with lightning impulse voltage. A big bowl shape electrode prepared with aluminum simulated a cloud. Experiments were performed with two electrode configurations, one the Cloud-rod electrode and the other cloud-needle with lightning impulse voltage generated by impulse generator. Probability of breakdown, time required for the propagation and propagation velocity were studied the measured results with the application of laser and without laser have been compared. A theoretical investigation has been made to estimate the minimum laser intensity required to ionize the atmospheric air. During the course of experimental investigations accurate measurement of magnitude of impulse voltage and propagation time were accomplished with the help of digital oscilloscope

For more details click here **back**

Title	***:***	***A Study Of Voltage Stability And VAR Need Of The Northern Regional Grid With Load Modeling***
Author(s)	***:***	***Sharma Ankush***
Supervisor(s)	***:***	***Sachchidanand& PrabhuS S***
Roll No	***:***	***9910412***

Abstract:

Over the past several years the problem of voltage stability has become a major concern for the large power networks like the Northern Regional Grid of India (NRGI). Load characteristics have considerable impact on system stability. In the present work voltage stability of NRGI is analyzed using load modeling. Mathematical model of load is integrated with AC-DC load flow to analyze system stability. Q-V modal analysis is utilized to determine critical modes associated with bus voltages for base case and contingencies. Bus participation factors are used to determine critical areas of the network, which require compensation. Fixed shunt compensations at selected buses are designed to keep bus voltages within reasonable range of ± 5% of nominal voltage. In areas where capacitors do not result in the desirable improvement in the associated modal voltage stability, SVC's are tried in their place. Ultimately, three SVC's are proposed for the network. The significant improvements achieved in voltage profile and stability of the compensated power system for base case and important contingencies are shown.

For more details click here **back**

Title : *Study Of Force-Commutated Converter Based HVDC System*

Author(s) : *Nitin Bansal*
Supervisor(s) : *Pal B C& Sachchidanand*
Roll No : *9910456*

Abstract:

This thesis investigates in detail the suitable configuration, appropriate control schemes and a few applications of a force-commutated converter based HVDC systems. Initially, starting from the fundamental principles, a suitable configuration (from the point of view of harmonic generation) of the force-commutated converters for HVDC application is determined. Subsequently, two different application of force-commutated converter based HVDC systems are considered, namely, a) interconnection of two AC systems and b) feeding of isolated loads. Appropriate control schemes are proposed for these two applications. The effectiveness of the proposed control schemes is validated through detail digital transient simulation using PSCAD/EMTDC software

For more details click here **back**

Title : *Study Of Lightning Effects And Protection Of Electronic Equipments*

Author(s) : *Jangid Ajay*

Supervisor(s) : *Arora Ravindra*

Roll No : *9910405*

Abstract:

For more details click here **back**

Title	***:***	***Experimental Investigations Of Electrically Stressed Droplets On Insulating Surfaces***
Author(s)	***:***	***Chaudhuri Balarko***
Supervisor(s)	***:***	***Arora Ravindra***
Roll No	***:***	***Y010405***

Abstract:

Experimental investigations were carried out to study the behaviour of discrete droplets on composite polymeric insulator surfaces. Mechanism of vibration of the droplets under an applied alternating electric field has been illustrated with the help of th e images obtained from high - speed camera recordings. The value of the voltage at which vibration in the droplets is just incepted has been measured for different volume and number of droplets having different arrangements. This value of voltage has been ob served to be capable of quantifying the insulator surface in terms of its hydrophobic properties. Field calculations have been performed and the experimental results were observed to be in perfect accordance with those obtained from simulation. Thus value of vibration inception voltage has been proved to be a qualitative estimate of the field enhancement in presence of droplets on insulating surfaces. The proposed method has been shown to be a non - destructive one for assessment of field enhancement. Mechani sm of collapse or merger of two droplets has been investigated along with the dependence of this phenomenon on droplet volume and insulator surface properties. Dependence of break - up or splitting of a single droplet on insulator surface properties, droplet volume and test voltage frequency has been determined. Variation of left and right contact angle under an applied electric field has been demonstrated for one half cycle. Effect of insulator material surface on the permanent elongation of the droplets aft er application of the electric field has been shown

For more details click here **back**

Title **:** ***Fuzzy Inference System Development For Refractory Brick Manufacturing Plant***

Author(s) **:** ***Kumar Mohan***

Supervisor(s) **:** ***Kalra Prem Kumar***

Roll No **:** ***Y010419***

Abstract:

The past few years have witnessed a rapid growth in the number and variety of applications of fuzzy logic. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support system, and portfolio selection. The basic concept underlying fuzzy logic is that of a linguistic variable, that is a variable whose values are words rather than numbers. Although words are inherently less precise than numbers, their use is closer to human intuition. Furthermore, computing with words exploits the tolerance for imprecision and thereby lowers the cost of solution. Another basic concept in fuzzy logic is that of a fuzzy if-then rule or, simply, fuzzy rule. Guiding principle of soft computing is to exploit the tolerance for imprecision, uncertainty, and partial truth to achieve tractability, robustness, and low cost solution. Among various combinations in soft computing, the one that has highest visibility is that of fuzzy logic. Hence the fuzzy logic toolbox of Matlab has been used to develop the fuzzy inference system for manufacture of converter lining bricks for Rourkela steel plant. Data mining tools such as CART (classification and regression trees) has been used for rule generation from data. Rule generation has also been done using Id3. validation of rules by use of Bayesian network and probabilistic study of effect of various parameters to predict final output has been done. Two systems have been developed one based on data and the other using expert advice for the rule generation.

For more details click here **back**

Title : *Expert System Development For Refractory Brick Manufacturing Process*

Author(s) : *Patil P A*
Supervisor(s) : *Kalra Prem Kumar*
Roll No : *Y010425*

Abstract:

Converters are a vital link in a steel plant and the plant productivity depends largely on the trouble free run of this steel - making vessel. Dramatic improvements have been made in converter life for a variety of reasons, which include, process development s, and developments in lining technology. Magnesia – Carbon refractories are one of the most researched subjects worldwide. Over the past years Rourkela Steel Plant, with the R&D centre for Iron and Steel, Ranchi has been successful in improving the lining life of its converter from 300 heats to 1000 heats, with considerable reductions in refractory cost per tonne of steel, and reductions in maintenance costs. To improve and sustain the lining life of converters an expert system is developed to predict var ious parameter and properties of the Magnesia - Carbon Bricks using the Flex software acquired by Steel Authority of India for this purpose. Two modules are developed one uses rules formulated from the advice of experts while the other uses rules derived out of plant data. Inductive Decision Tree (ID3) algorithm for rule generation is also used and discussed. The results from both the modules are compared with the result of Matlab Fuzzy Toolbox. Tools like Microsoft Bayesian Network and Multavariate Adaptive Regression spli

For more details click here **back**