A Novel Method for Synchronization with Unbalanced Grid: An Experimental Investigation

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***Abstract*—A major issue for the grid connected renewable energy system specifically during unbalance grid condition is the grid synchronization. Under unbalance grid condition, in order to implement stable operation, it is necessity to determine the grid parameter accurately and rapidly. Algorithms used for Grid synchronization plays an important role in the control and steady operation of grid-connected converters. To implement stable and steady control strategy under unbalance grid condition,the detection of grid parameter accurately and rapidly are also crucial. Synchronous Reference Frame Phase Locked Loop (SRF-PLL) works satisfactory for balance grid condition but its performance deteriorates with unbalance grid condition. However, Dual Second Order generalized Integrator (DSOGI)-PLL performs reasonably well in grid synchronization during unbalance grid condition. DSOGI consists of a low pass lter (LPF) and band pass lter to attenuate harmonic of the unbalance grid. In SRF-PLL, the angle is tracked in such a way that the maximum phase voltage is reflected on d-axis while component voltage along q-axis is zero. Hence taking the advantages of DSOGI and SRF-PLL, the DSOGI-PLL architecture has been proposed in this paper. The proposed DSOGI-PLL has better performance in grid synchronization under unbalance grid conditions.**

I. INTRODUCTION

The sinusoidal behavior of the grid voltage are easily observed under balance operating conditions. The nature of distortion and unbalance can noticed when grid is subjected to fault, unbalance and nonlinear loads. Under these conditions, converters with grid-tied mode are desired to remain connected with the grid to support the grid called low voltage ride through (LVRT). To support the LVRT the grid synchronization has an important role.

Phase Locked Loop is a circular loop which is formed by the feedback. In general it used to lock the input signal frequency and phase with estimated one. The main motivation of the PLL is to generate a signal whose phase and frequency matches with the reference signal. The bandwidth of the locking signal should be in the range of PLL. The feedback loop is continued until the phase and frequency of the signal is locked with the reference signal. In three-phase ideal systems, synchronous reference frame-PLL (SRF-PLL) for grid synchronization technique is widely used due to its accuracy and fastness. But during unbalance grid condition the fastness and accuracy decreases due to presence of negative sequence component. In order to overcome this problem, many scholars have proposed different advanced algorithm for grid synchronization. Zero crossing-detection-based methods [1], Kalman ltering [2], sliding discrete Fourier transform and its modification [3] recursive weighted least squares estimation algorithms [4], artificial neural networks [5], concept of adaptive notch lter [6] and phase-locked loop (PLL)based algorithms [7] are among the existing synchronization technique available in the literatures.

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Due to large computational effort and high complexity Hilbert transformation-PLL(HTPLL) [8] is not a preferable. The handling of accumulated error is very crucial in SDFT-PLL [9]. The limiting harmonic filtering capability make Differentiation PLL [10], All Pass based Filter-PLL [11] and Synthesis Circuit-PLL [12] is not preferable during unbalance grid condition. In [10] and [13] a new design rule to reduce the second-harmonic ripples is presented.

However, under varying frequency conditions it is not possible to achieve zero steady-state error as it does not eliminate the second-harmonics completely. In this paper, a new approach has been proposed using SOGI-PLL instead of conventional SRF-PLL is proposed. This method has an effective elucidation for grid synchronization under unbalance grid conditions. The proposed synchronization system is examined in Matlab/Simulink platform and its hardware validation is carried out on dSPACE-1104 platforms.

II. BASIC KNOWLEDGE OF SRF-PLL

Under normal grid conditions the performance of the SRF-PLL is satisfactory.The SRF-PLL consists of rotating frame transformation. Here the transformation of the three-phase voltages,and the angle is done by keeping synchronous with the grid phase voltage. The revolution is done in such a way that at steady state the occasioning V_q voltage is set to zero volt and V_d will represent maximum phase voltage. To realize this

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one a proportional integral controller is used. Fig. 2 illustrates the basic structure of SRF-PLL.

The transformation of rotating reference frame from stationary reference frame as follows

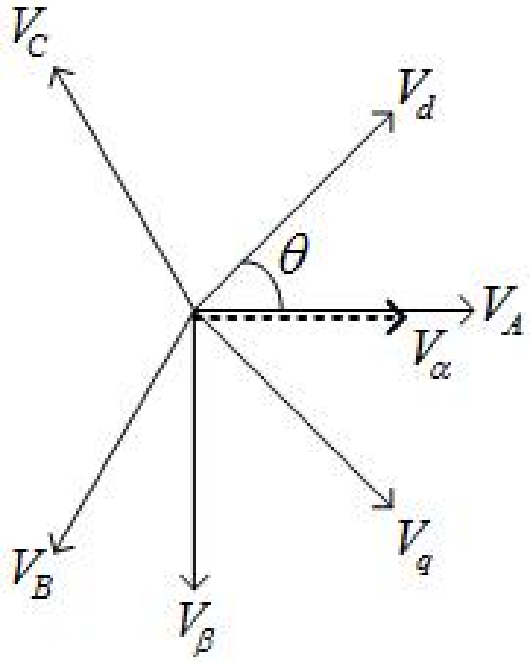

Fig. 1: Phaser digram representation of Orthogonal Signal

$$V_{dq} = V_d + jV_q \tag{1}$$

$$V_{\alpha\beta} = V_\alpha + jV_\beta \tag{2}$$

$$V_{dq} = \left[e^{j\theta}\right] \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3}$$

$$V_d = V_m \cos\left(\hat{\theta} - \theta\right) \tag{4}$$

$$Vq = V_m \sin\left(\hat{\theta} - \theta\right) \tag{5}$$

$$V_\alpha = V_m \cos\left(\theta\right) \tag{6}$$

$$V_\beta = V_m \sin\left(\theta\right) \tag{7}$$

where Vm represents the peak of the phase voltage. and $\hat{\theta}$ is the deviation from original grid angle.
When

$$\hat{\theta} = \theta \tag{8}$$

and

$$\theta = \omega t, \tag{9}$$

then

$$V_d = V_m, \quad , \tag{10}$$

$$Vq = 0, \tag{11}$$

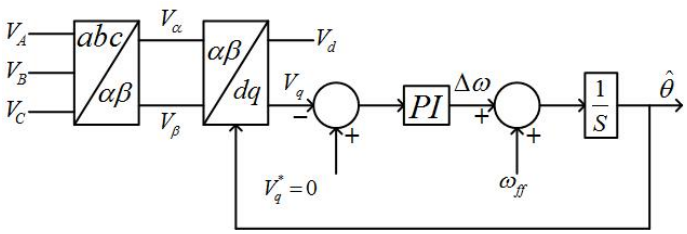

Fig. 2: Basic structure of PLL

The open loop transfer function of the above one will be:

$$G(S) = \left(\frac{SK_p + K_i}{S}\right)\left(\frac{1}{1 + ST_s}\right)\frac{V_m}{S} \tag{12}$$

Here in the PI tunning K_p=3.85 K_i=611.85 and T_s is the sampling time.

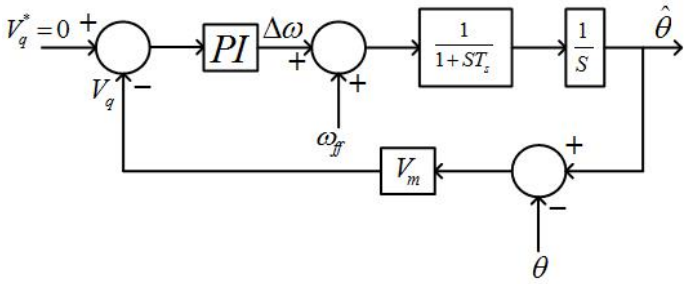

Fig. 3: Small signal model for Control structure for PLL

During unbalanced grid condition,the existence of negative sequence component can be realized. As a result the output waveform of the dq transformation consists a ripple of double the fundamental frequency component. On the basis of PLL bandwidth window, this ripple gets enervated however these circulated in the loop and possesses errors in calculable frequency and angle θ. This causes the output waveform in distortions condition. The distortion can be resolved in terms of amplitude (THD) and phase angle difference in terms of tracing of the positive sequence of the input voltage. The disadvantages of PLL is that it is unable to track the angle and frequency during unbalance condition.

A. Unbalance Grid

Let a three phase voltage V_A,V_B and V_C having unequal magnitude.The stationary reference frame transformation gives signal V_α and V_β

$$V_\alpha = V_A - \left(\frac{V_B + V_C}{2}\right) \tag{13}$$

$$V_\beta = \frac{\sqrt{3}}{2}\left(V_B - V_C\right) \tag{14}$$

$$V_\alpha = V_x \sin\left(\omega t + \psi_1\right) \tag{15}$$

$$V_\beta = V_y \sin\left(\omega t + \psi_2\right) \tag{16}$$

$$\hat{\theta} = \omega t + Z \tag{17}$$

$$Z = A\sin(2\omega t + \psi) \quad (18)$$

$$V_q = V_\alpha \sin\left(\hat{\theta}\right) + V_\beta \cos\left(\hat{\theta}\right) \quad (19)$$

$$V_q = V_x \sin(\omega t+\psi_1)\sin(\omega t+Z)+V_y \sin(\omega t+\psi_2)\cos(\omega t+Z) \quad (20)$$

This Vq term is subtracted from zero feed to a PI controller in order to minimized the steady state error. The output of the PI controller is add with fed-forward term ω_{ff} in order to take care of the frequency oscillation. After this one, this is followed by a loop filter with an integrator.

III. MATHEMATICAL DESCRIPTION

A three phase unbalance system can be represented as:

$$V_A = 1\sin(\omega t) \quad (21)$$

$$V_B = 0.2\sin(\omega t - 2 * pi/3\ ) \quad (22)$$

$$V_C = 0.5\sin(\omega t + 2 * pi/3\ ) \quad (23)$$

This above three phase voltage signals are transformed into stationary $\alpha\beta$ reference frame in terms of V_α and V_β. These two signals are passes through two SOGI blocks in order to produce two set of orthogonal signal which are shown in Fig.1.

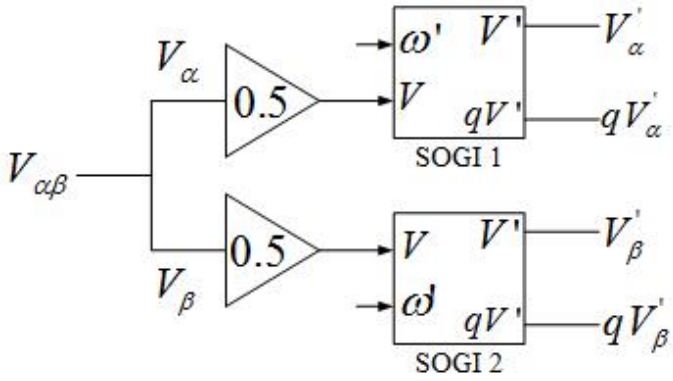

Fig. 4: Generation of Orthogonal signal from Stationary frame

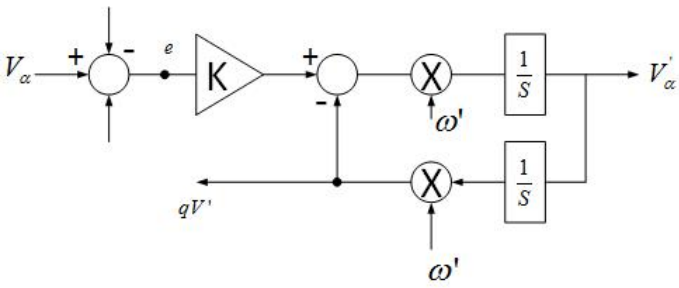

Fig. 5: Basic structure of SOGI

These voltage signals are used to synthesize the set of positive sequence component and negative sequence components by proper mathematical operations and represented as follows.

$$V'_\alpha - qV'_\beta = V_\alpha^{PS} \quad (24)$$

$$V'_\beta + qV'_\alpha = V_\beta^{PS} \quad (25)$$

$$V'_\alpha + qV'_\beta = V_\alpha^{NS} \quad (26)$$

$$V'_\beta - qV'_\alpha = V_\beta^{NS} \quad (27)$$

These stationary reference frame quantities are converted into rotating reference frame by adjusting θ (extracted from PLL) in such a way that maximum amplitude phase voltage is reflected on d-axis whereas voltage component along q-axis remains zero as shown.

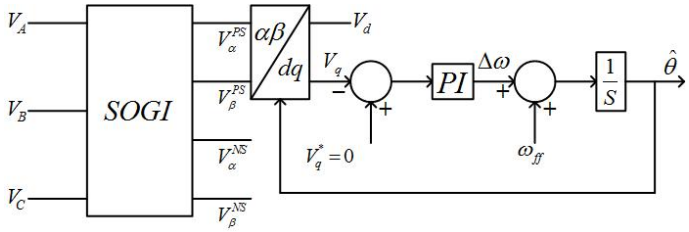

Fig. 6: Control structure of SOGI-PLL

Fig.6 elucidates the control structure of the SOGI-PLL. It's transfer functions is based on quadrature signal generator (QSG).

The block diagram of SOGI is shown in Fig.5 and its transfer function is:

$$G(S) = \frac{V'_\alpha}{V_\alpha}(S) = \frac{S\omega'}{S^2 + \omega'^2} \quad (28)$$

From equation (28), it is established that the SOGI filter consists of an infinite-gain integrator with sinusoidal input signal at fundamental frequencies. It also manifests that the system shown in Fig. 5, consists of a band pass filter and a low pass filter. The transfer functions of such system can be written as:

$$A(s) = \frac{V'_\alpha}{V_\alpha}(S) = \frac{C\omega' S}{S^2 + C\omega' S + \omega'^2} \quad (28)$$

$$B(S) = \frac{qV'}{V_\alpha}(S) = \frac{C\omega'^2}{S^2 + C\omega' S + \omega'^2}, \quad (29)$$

Where C and ω' are the damping factor and resonant frequency respectively. Here C is taken as 1.414 and ω' is taken as 314 rad/sec. The transfer functions of (28) and (29) consists of band-pass and low-pass filter respectively, which has the capability to eliminate harmonics of the input signal V. It is also proved that if the input signal V is a sinusoidal signal and V_α^{PS} is in phase with V_α and V_β^{PS} is in phase with V_β. During unbalance grid the frequency and phase angle changes. As result the response of $A(S)$ and $B(S)$ changes which indicate the presence of negative sequence in the rotating reference frame which appears at double the fundamental frequency as a steady state error.

The job of PI controller is to maintain the reactive component of voltage V_q set to zero value and also regulate the angular velocity of the of the rotating system dq. The speed of virtual rotation of the dq system depends on resulting angular

velocity ωPLL. Since the maximal range of supply voltage frequency is expected to vary from 48Hz to 52Hz. So the PI tuner is realized with symmetrical saturation limiter whose value is set to ± 2 Hz.

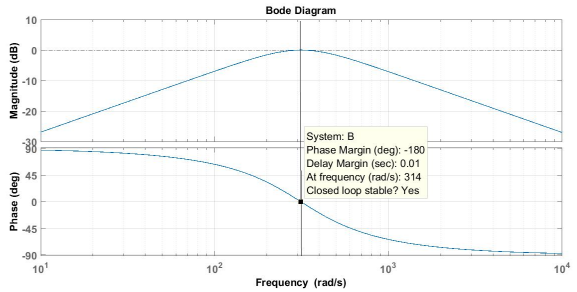

Fig. 7: Frequency response for Band-pass filter

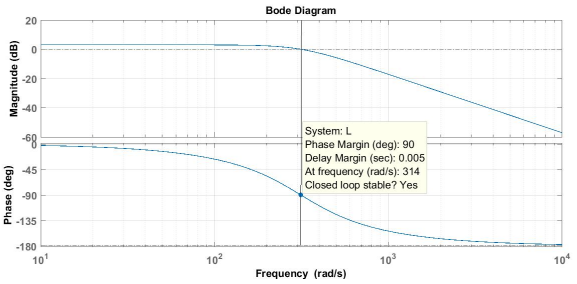

Fig. 8: Frequency response for Low-pass filter

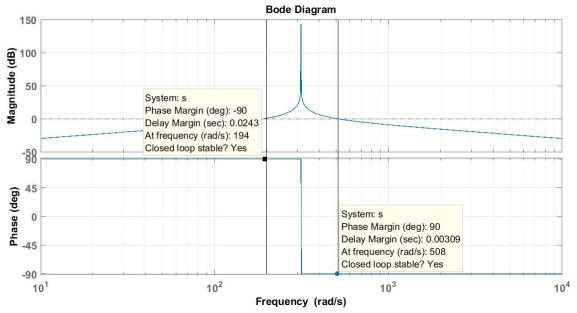

Fig. 9: Frequency response for SOGI

Here it is found that the bandwidth of SOGI-PLL is varies from 194 rad/sec to 508 rad/sec. It implies that the range of operation is 314 rad/sec which indicate SOGI-PLL is capable to eliminate the double frequency component during disturbance as it is shown in Fig. 9. It is also examined that the output signal is in phase with the fundamental frequency from Fig. 7 where as in Fig. 8 represents that the input signal is having a 90° phase shift with the fundamental frequency.

IV. EXPERIMENTAL SETUP

An experimental prototype is built in the laboratory on dSPACE- 1104 platform as shown in Fig. 10. Three phase unbalanced voltage profile has been created with amplitudes

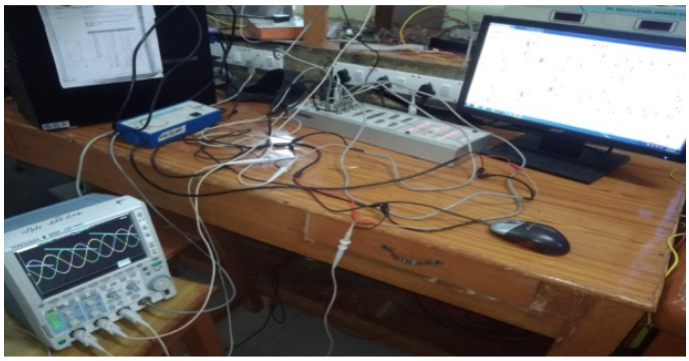

Fig. 10: An Experimental Setup

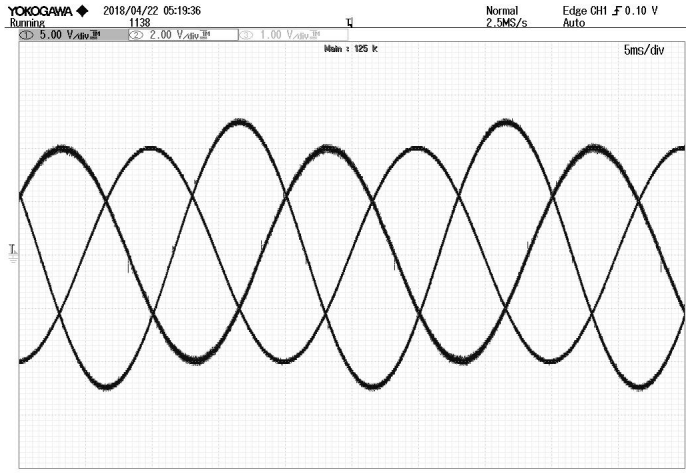

Fig. 11: Three phase Unbalance voltage profile

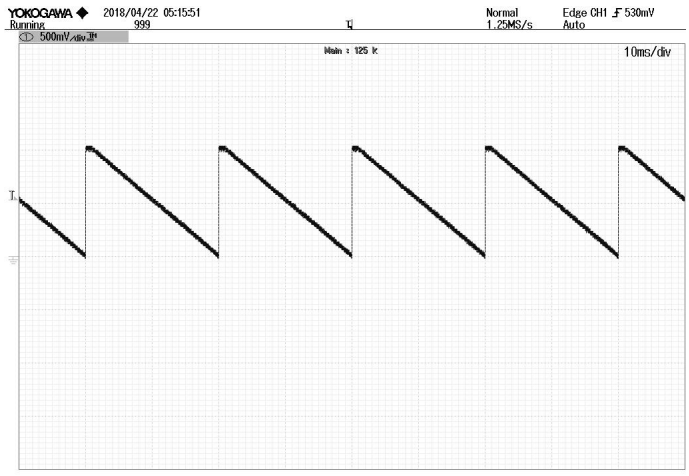

Fig. 12: Extraction θ from SOGI-PLL

of 1, 0.5 and 0.2 with phase displacement of 120° among these signals in. Through DAC port these signals are carry out from the dSPACE and again fed into the dSPACE domain through ADC port to have real time testing of the proposed algorithm.

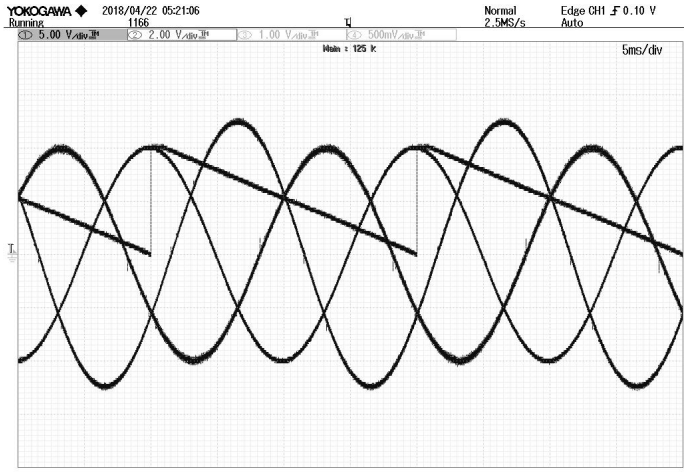

Fig. 13: Synchronization of theta with unbalance voltage

These three signals are transformed to $\alpha\beta$ domain and again converted to dq domain by using the θ extracted from DSOGI-PLL. The unbalances of three phase voltages are shown in Fig. 11. Here A- phase voltage is having magnitude of 10 V, B-phase voltage having 4 V and C-phase is having 2.5 V. Due to scaling factor of 10. Fig. 12 shows outcome of DSOGI-PLL and the synchronization of grid angle with the unbalance grid is presented in Fig. 13. It is observed that our reference frame is rotating in opposite direction so the output of PLL is oriented according to it.

V. CONCLUSION

Here it is observed that the DSOGI-PLL is a robust one to track the θ of the unbalanced grid perfectly ensuring grid synchronization of the grid-tied inverter.

VI. ACKNOWLEDGMENT

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REFERENCES

[1] F. D. Freijedo, J. Doval-Gandoy, Ó. LÓpez, and E. Acha, "A generic open-loop algorithm for three-phase grid voltage/current synchronization with particular reference to phase, frequency, and amplitude estimation," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 94–107, 2009.

[2] J. Svensson, "Synchronisation methods for grid-connected voltage source converters," *IEE Proceedings-Generation, Transmission and Distribution*, vol. 148, no. 3, pp. 229–235, 2001.

[3] P. Sumathi and P. A. Janakiraman, "Integrated phase-locking scheme for sdft-based harmonic analysis of periodic signals," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 1, pp. 51–55, 2008.

[4] M. D. Kusljevic, J. J. Tomic, and L. D. Jovanovic, "Frequency estimation of three-phase power system using weighted-least-square algorithm and adaptive fir filtering," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 2, pp. 322–329, 2010.

[5] L. Lai, W. Chan, C. Tse, and A. So, "Real-time frequency and harmonic evaluation using artificial neural networks," *IEEE Transactions on power delivery*, vol. 14, no. 1, pp. 52–59, 1999.

[6] L. Hsu, R. Ortega, and G. Damm, "A globally convergent frequency estimator," *IEEE Transactions on Automatic Control*, vol. 44, no. 4, pp. 698–713, 1999.

[7] F. D. Freijedo, A. G. Yepes, O. Lopez, A. Vidal, and J. Doval-Gandoy, "Three-phase plls with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 85–97, 2011.

[8] P. Hao, W. Zanji, and C. Jianye, "A measuring method of the single-phase ac frequency, phase, and reactive power based on the hilbert filtering," *IEEE Transactions on Instrumentation and Measurement*, vol. 56, no. 3, pp. 918–923, 2007.

[9] P. Sumathi and P. A. Janakiraman, "Integrated phase-locking scheme for sdft-based harmonic analysis of periodic signals," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 1, pp. 51–55, 2008.

[10] P. Lamo, F. López, A. Pigazo, and F. J. Azcondo, "An efficient fpga implementation of a quadrature signal-generation subsystem in srf plls in single-phase pfcs," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3959–3969, 2017.

[11] S. Golestan, J. M. Guerrero, A. Abusorrah, M. M. Al-Hindawi, and Y. Al-Turki, "An adaptive quadrature signal generation-based single-phase phase-locked loop for grid-connected applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2848–2854, 2017.

[12] X. Fang, Y. Wang, M. Li, and J. Liu, "A novel frequency-adaptive pll for single-phase grid-connected converters," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*. IEEE, 2010, pp. 414–419.