Experimental Validation of CCM and DCM Operations of Semi-Bridgeless Boost Rectifier for Power Quality Improvement in UPS System

S. Rajasekar, *Member IEEE*
Senior Research Engineer,
Technology Development Department
Powergrid Corporation of India Limited
Gurgaon, Haryana, India
rajasekar@powergridindia.com

V. Karthikeyan, *Member IEEE*
Assistant Professor,
Dept. of Electrical Engineering
National Insitutue of Technolgy
Calicut, India
karthikeyan@nitc.ac.in

N. Kumaresan, *Senior Member IEEE*
Professor,
Dept. of Electrical and Electronics Engg.,
National Insitutue of Technolgy
Trichy, India
nkumar@nitt.edu

***Abstract*—This paper discusses experimental validation of semi-bridgeless boost rectifier (SBBR) operation of continuous conduction mode (CCM) & discontinuous conduction mode (DCM) for power quality improvement in uninterrupted power supply (UPS) system. The double stage conversion in UPS attenuates power quality at the input side and output configuration of the system. Many researchers have proposed the improvement of power quality with CCM and DCM operations for ac-dc conversion stage in bridge and bridgeless rectifier, but there is lack of knowledge about their performance and drawbacks of CCM and DCM operation with SBBR topology. This paper focuses on experimental analysis of SBBR topology operating in CCM and DCM under different load ranges. The performance of power quality factors and efficiency of SBBR operating in CCM and DCM are addressed. To study the stability analysis of SBBR operation in CCM and DCM, a comprehensive small signal model is derived by analyzing the inductor current waveforms. PSCAD simulations have obtained theoretical study of SBBR with CCM and DCM operations and experimental validation is carried out through FPGA Spartan 3A processor**.

Keywords—conduction mode, continuous conduction mode, discontinuous conduction mode, semi-bridgeless boost rectifier, uninterrupted power supply.

I. INTRODUCTION

Uninterrupted power supply (UPS) for critical electrical systems has become main stream in all industries due to continuous power requirement by load. Generally, UPS is inevitable to safeguard the sensitive loads from wide variations in voltage and power outages. But, the benefit of UPS is accompanied with a major drawback which is the power loss due to double conversion stage. Hence the power quality needs to be improved [1].

Basically, ac-dc rectifier followed by filter capacitor to hold stable output results in poor power factor (PF), high crest factor (CF) and high input current harmonic distortion. The input current waveforms are non-sinusoidal and peaky with short interval in a half cycle. The non-linearity of input current in UPS system causes several drawbacks such as high total harmonic distortion (THD), current stress, thereby reducing the efficiency and thermal performance [2]-[5]. For the past 20 years, the issues in power quality at input side and its improvement using dc-dc converters are discussed [6-8]. There are several dc-dc converters proposed to improve power factor (PF) [9]. The most popular power factor correction (PFC) converter is boost converter and it contains single switch and diode. To improve system efficiency, the bridgeless boost converter topology has been proposed [10]-[12]. The semi-bridgeless boost rectifier (SBBR) has been introduced to achieve higher performance in power quality parameters [13]. The significant feature of SBBR is that there is no interference occurrence due to two separate inductor plays at every half cycle of operation. The current ripple EMI filter requirement is minimized when adopting two or three phase interleaved stage. Hence, for practical implementation and problem troubleshooting, the SBBR is easier than bridgeless converter [14]-[15]. The various PFC control techniques are used in which constant frequency PWM technique is simpler for bridge type and bridgeless PFC boost converter. Also, the output voltage can be easily adjusted with better power quality [16].Hysteresis current control ensures that better control mechanism for dynamic load conditions and switching control signal makes variable bandwidth in each half cycle in spite of its symmetry [17].

While designing the PFC based ac-dc converter, the designer must have clear information about various modes of operation, such as DCM, CCM and BCM. Although many authors have been focused on better power quality with CCM and DCM operating modes in ac-dc conversion stage in conventional bridge type rectifier and bridgeless rectifier, there is still lack of knowledge about CCM and DCM operation with SBBR [18]-[20]. Inductor current ensures DCM due to its non-linearity at light load case. Inaccurate average current is sensed which results in delayed zero crossings. CCM and DCM occur in each ac half cycle. The inductor current (i_L) ensures DCM operations and the inductor peak current ensures the operations of CCM. DCM brings non linearity behaviours of inductor current, whereas, CCM brings linearity behavioural. It is essential to reduce current distortion by maintaining acceptable good input current during light load to heavy load.

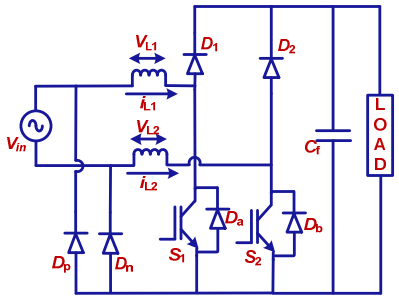


Fig. 1 Basic topology of semi-bridgeless boost rectifier

This paper particularly focuses on experimental analysis of SBBR with CCM and DCM operations in power quality improvement at input side for UPS system at different load ranges.

978-1-5386-6159-8/18/$31.00 ©2018 IEEE

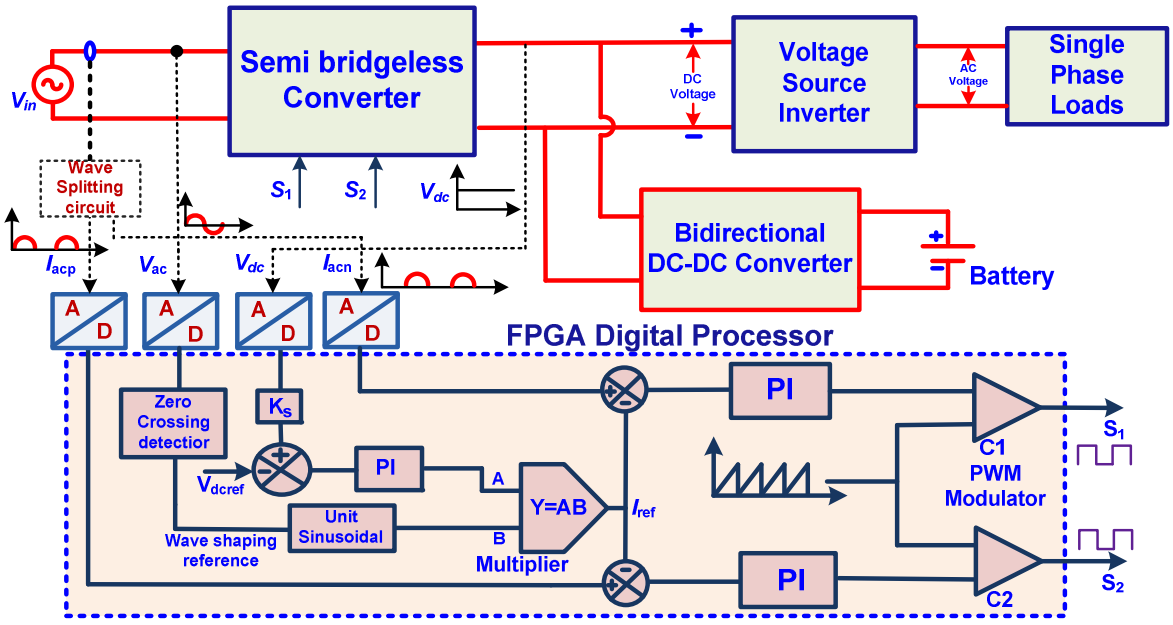


Fig. 2 Generalized block diagram of semi-bridgeless boost rectifier fed online UPS system with digital controller

To improve the power factor the delay in zero crossings is eliminated and the digital control is implemented through VHDL coded FPGA processor. The basic topology of SBBR is shown in Fig.1 and it has additionally two fast recovery diodes different than conventional bridge type dc-dc converter named d_1 and d_2 respectively. In each half cycle interval, inductor stores and retrieves the energy through respective switches S_1 and S_2 and d_1 and d_2, respectively.

II. Basic Approach of PFC in SBBR

The generalized block diagram of SBBR fed by online UPS system with digital controller is shown in Fig. 2. It comprises three units: SBBR, voltage storage inverter and bidirectional DC-DC converter with battery storage unit. This paper particularly focuses on PFC and THD improvement in SBBR units. Conventional CCM operations are replaced by DCM operations to accomplish better quality [20]–[23]. However, the higher current results in stress both active and passive components, which leads higher losses. The control block diagram of SBBR for switching signal generation to S_1 and S_2 is represented as Fig. 2. The source voltage and current are sensed and the voltage wave is separated through wave splitting circuit. The error signal is obtained by comparing actual with reference DC voltage and further processed into PI controller.

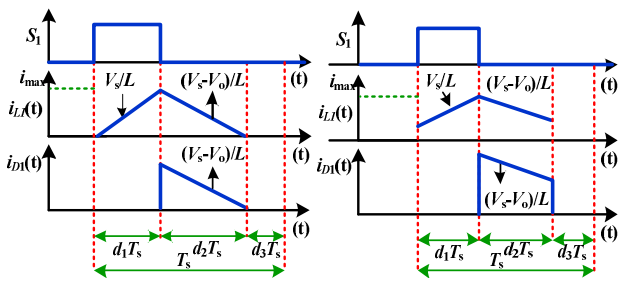


Fig.3 Inductor and diode current waveform, (a) DCM operation (b) CCM operation

The digital zero crossing detection is employed by using FPGA processor to attain unity power factor, which enables or disables the PI output to produce PWM signal.

PWM pulse is generated by comparing the PI controller output signal with unit sine wave signal.

III. Stability of DCM/CCM Mode of Operation

This section presents the operation of CCM and DCM for SBBR. Fig. 3(a) and (b) depicts the boost inductor (L_1) and diode (D_1) current waveform for one switching period (T_s) of bridgeless dual boost converter for DCM and CCM operation, respectively with $d_1+d_2 < 1$ The turn on time is denoted as d_1T_S, d_2T_S the inductor current discharging and (d_2+d_3) T_S is the turn off time. The small signal model of the bridgeless PFC dual boost converter is derived to perform the stability analysis in this section. The magnitude of ac input voltage is assumed to be constant in the switching period T_s and it is replaced by an equivalent voltage source of magnitude equal to nominal value of RMS voltage [27]. The following steps are used to derive the small signal modelling of converter, which ensure validity of transfer function obtained up to $f_s/2$.

The averaged equation for this converter is:

$$L\frac{di_{L-avg}}{dt} = d_1V_s + d_2(V_s - V_o) \quad (1)$$

From Fig. 3(a), the average inductor and diode current comes out to be:

$$i_{L-avg} = \frac{i_{L-\max}}{2}(d_1 + d_2) \quad (2)$$

$$i_{D-avg} = \frac{d_2^2T_s^2}{2L}(V_o - V_s) \quad (3)$$

The peak inductor current is equal to:

$$i_{L-\max} = \frac{V_{rms}}{L}d_1T_s \quad (4)$$

Substituting (4) in (2), we get the relation between d_1 and d_2.

$$d_2 = \frac{2Li_{L-avg}}{d_1T_sV_s} - d_1 \quad (5)$$

Further, from (5) we obtain

$$L\frac{di_{L-avg}}{dt} = \frac{2Li_{L-avg}}{d_1T_s}\left(\frac{V_s - V_o}{V_s}\right) + d_1V_o \quad (6)$$

Eqn. (6) is literalized about the nominal operating point and after introducing perturbation in the steady state values, inductor current transfer function is obtained as:

$$G_{DCM}(s)=\frac{\hat{i}(s)}{\hat{d}(s)}=\frac{V_o}{L}\frac{2}{s+2\sqrt{\frac{(V_o/V_s-1)V_o}{2LI_LT_s}}} \quad (7)$$

Another representation of the average inductor current when (4) is substituted in (2) is:

$$i_{L-avg}=\frac{V_s}{2L}T_s d_1(d_1+d_2) \quad (8)$$

We can infer the inductor current ripple during charging and discharging period is equal, which gives as,

$$\frac{T_s d_1}{L_1}V_s=\frac{T_s d_2}{L_1}(V_o-V_s) \quad (9)$$

$$d_2=\frac{V_s}{(V_o-V_s)}d_1 \quad (10)$$

Substituting (10) in (3) provides the following:

$$i_{D-avg}=\frac{V_s^2 d_1^2 T_s}{2L(V_o-V_s)} \quad (11)$$

$$i_{L-avg}=\frac{V_s d_1^2 T_s}{2L}\left(\frac{V_o}{V_o-V_s}\right) \quad (12)$$

By adopting the same procedure of introducing small ac perturbation in the variables of (11), (12) the following small signal equations:

$$\hat{i}_L=\frac{T_s}{2L}\left(g_1\hat{d}_1+j_1\hat{v}_o+\frac{1}{r_1}\hat{v}_m\right) \quad (13)$$

$$\hat{i}_D=\frac{T_s}{2L}\left(g_2\hat{d}_1-\frac{1}{r_2}\hat{v}_o+j_2\hat{v}_m\right) \quad (14)$$

Here,

$$g_1=\frac{2V_sV_o}{(V_o-V_s)}\quad j_1=\left(\frac{V_sD_1^2-I_L}{V_o-V_s}\right)\quad \frac{1}{r_1}=\left(\frac{V_oD_1^2-I_L}{V_o-V_s}\right) \quad (15a)$$

$$g_2=\left(\frac{2D_1V_s^2}{V_o-V_s}\right)\quad j_2=\left(\frac{2D_1V_s^2+I_D}{V_o-V_s}\right)\quad \frac{1}{r_2}=\left(\frac{I_D}{V_o-V_s}\right) \quad (15b)$$

Utilizing the above derived small signal equations, the control to output transfer function is determined as,

$$\left(\frac{\hat{v}_o}{\hat{d}}\right)_{\hat{d}_1=0}=\frac{g_2}{\left(j_2+\frac{1}{R}+Cs\right)} \quad (16)$$

The small signal transfer function ratio between CCM duty cycle control and output voltage is given as:

$$\frac{\hat{v}_o}{\hat{d}}=\frac{I_{L-CCM}}{\left(Cs+\frac{1}{R}\right)} \quad (17)$$

The transfer function ratio between inductor current and duty cycle control is derived using [28]:

$$\frac{\hat{i}_L(s)}{\hat{d}(s)}=\frac{(CV_o)s+2(1-D)I_L}{(LC)s^2+\frac{L}{R}s+(1-D)^2} \quad (18)$$

Where, D is the duty cycle of PWM signal.

Fig. 4 and Fig. 5 depict the frequency response of control to inductor current transfer function operating in CCM and DCM respectively.

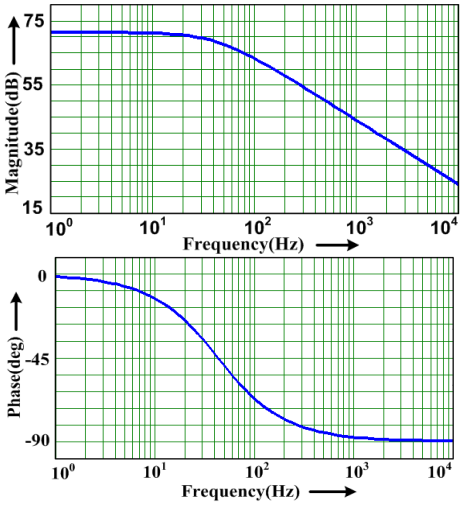


Fig. 4 Bode plot of change in inductor current with change in *d* at DCM

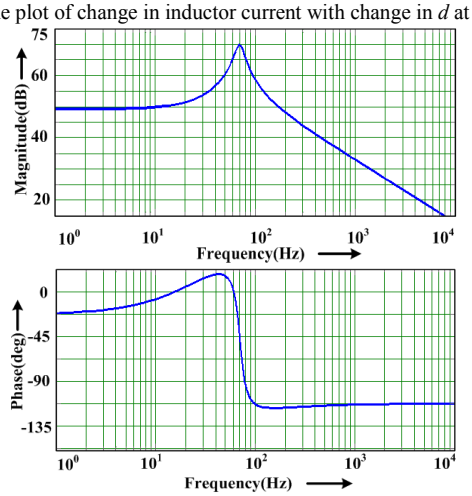


Fig. 5 Bode plot of change in inductor current with change in *d* at CCM

There is a large peak in magnitude plot and phase margin becomes negative at that frequency where condition of resonance is achieved since it is an uncompensated system. As duly mentioned in [2], the present DCM model can be used to extract a bandwidth greater than $2fL$ from the closed loop system. At frequencies greater than $2fL$ the system is inherently stable as the gain margin exhibited by two small signal transfer functions is equal to infinity. Sufficient inherent phase margin decreases requirements on the controller. The range of frequencies includes the low line frequency (50/60Hz) and the high switching frequency of the converter (10 kHz).

IV. Analysis of Simulation and Experimental Results

To compare the performance of DCM and CCM in SBBR, simulation and experimental validations are discussed in this section. In order to demonstrate the method and analysis of PFC converter, the SBBR specifications are displayed in Table 1. The SBBR is configured with IRFP250N-MOSFET and HUR3060-Fast recovery diodes. These switches are turned on according to the input sine wave signal obtained through zero crossing detectors. For steady state performance evaluation, V_{ac} is fixed and two identical inductor values have been considered.

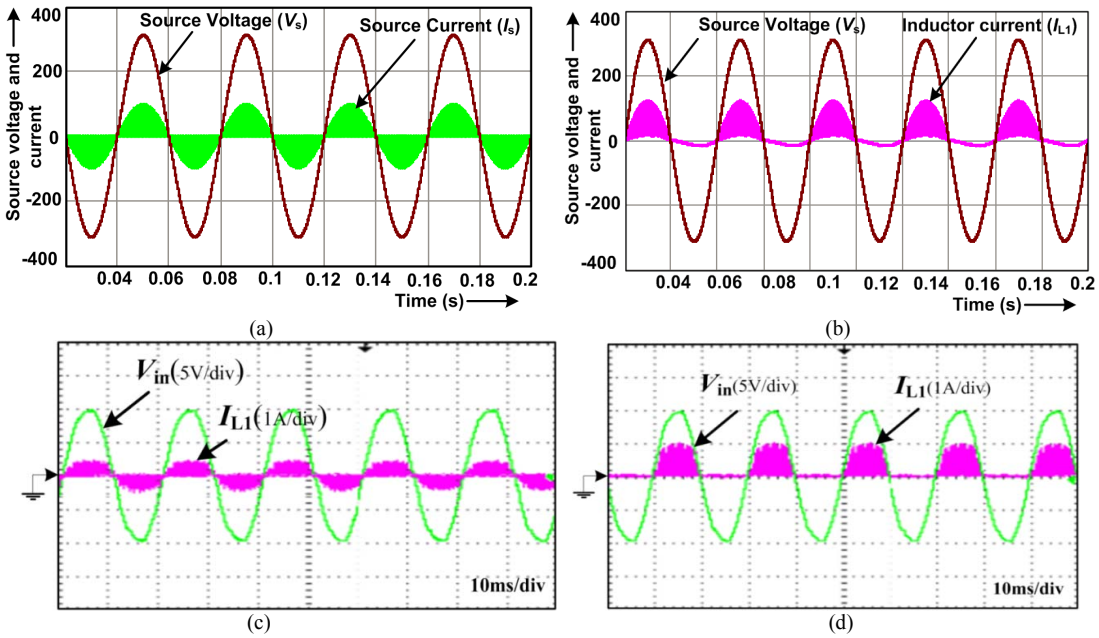


Fig. 6 Results in DCM operation (a) simulation result of source voltage and current (b) simulation result of source voltage and inductor current (c) Experimental result of source voltage and current, (d) Experimental result of source voltage and inductor current.

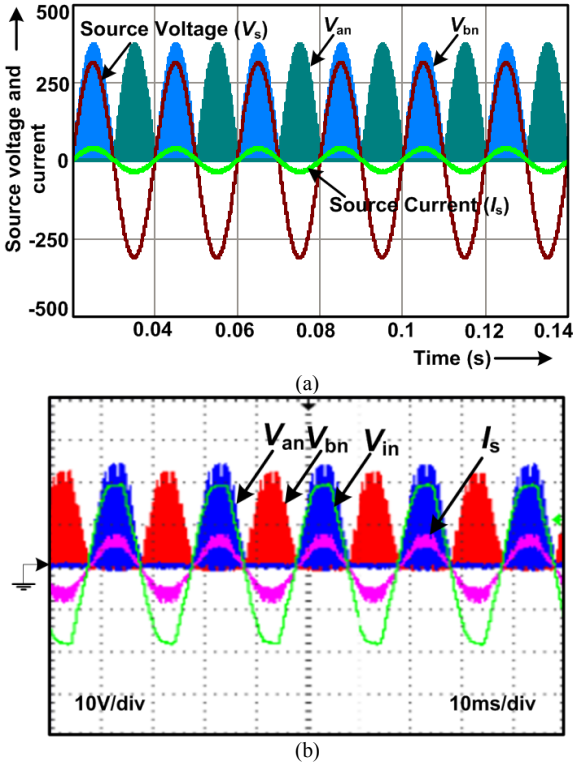
TABLE 1
SIMULATION AND EXPERIMENT SETUP PARAMETERS

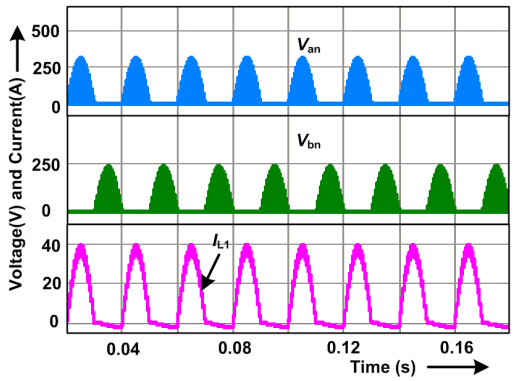
Parameter	*Simulation*	*Experiment*
Inductance (L_1 and L_2)	1 mH	10 mH
Switching Frequency	20 kHz	20 kHz
Input voltage	220 V	15 V
Output capacitance	1000 µF	220 µF

The power factor significantly improved in DCM and the simulation results are represented in Fig. 6. The results of source voltage and its corresponding source current are depicted in Fig. 6(a). During positive half cycle, the inductor current (I_{L1}) in DCM operation is displayed in Fig. 6(b). From this we can infer a small amount of current circulating through L_1. To validate the performance of SBBR in DCM operations, the experimental results also observed and depicted in Fig. 6 (c) and (d).

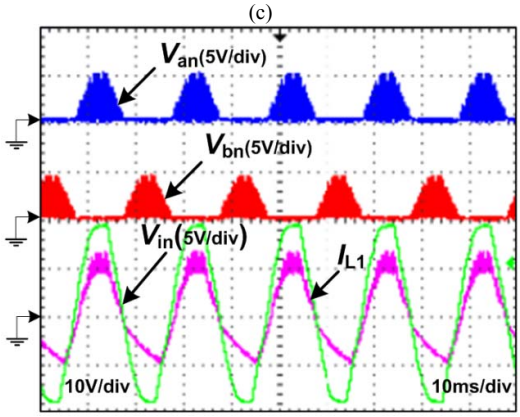
Fig. 6(c) shows the response of the source current following in phase with the source voltage and the inductor current in positive half is captured and shown in Fig. 6(d). It is demonstrated from these results that the peak current of inductor is larger in DCM operation and resulting to higher switching stress than CCM operation. In addition, PF is improved and THD is reduced. Therefore, enhanced power quality is accomplished. Simulation and experimental validation results in CCM mode are depicted in Fig. 7 and 8. The source current, voltage and voltage across the switches are displayed in Fig. 7(a). The SBBR performs AC-AC boost operation with rectification, and the voltage across the switch S_1 and S_2 are called as Van and V_{bn}, respectively. The peak voltage of Van and V_{bn} are determined by the duty cycle of S_1 and S_2. Fig. 7(b) shows the inductor current in CCM operation and it is observed from the waveform the peak current of inductor is less compared to inductor current at DCM operation at same load condition.

Fig. 7(c), represent the source voltage and current waveforms captured in laboratory experimental setup. Fig. 7(d) depicts positive half cycle inductor current and its corresponding voltage across the switches i.e., S_1 and S_2.The inductor current charges and discharges according to voltage appearing across the switch. In steady state condition experimental results of source voltage (V_{an}, V_{bn}) and source current are represented in Fig. 8. Simulation and experimental validation result are closely matches in both DCM and CCM. From the power quality views, the power factor and THD are quite better in DCM operation than CCM, but the current stress of the inductor is higher. To conclude the performance of SBBR in terms of power quality, the graph for power factor with respect to change in load condition for DCM and CCM is shown in Fig. 9(a). The power factor in CCM is quite better than DCM operation. The input current THD under load variations are plotted in Fig. 9(b). It is worthy to note the input current THD < 5% under 50% of rated load condition and it is acceptable as per IEC 61000-3-2 standards.





(c)



(d)

Fig. 7 Results in CCM operation (a) simulation result of source voltage and current (b) simulation result of source voltage and inductor current (c) Experimental validation result of source voltage and current, (d) Experimental validation result of source voltage and inductor current

After observing these results, it shows the power quality performance of SBBR in DCM operation is better than CCM operation. The efficiency graph with variation of load for CCM and DCM operations are shown in Fig. 10. The efficiency in CCM is slight higher than DCM operation due to lesser peak current.

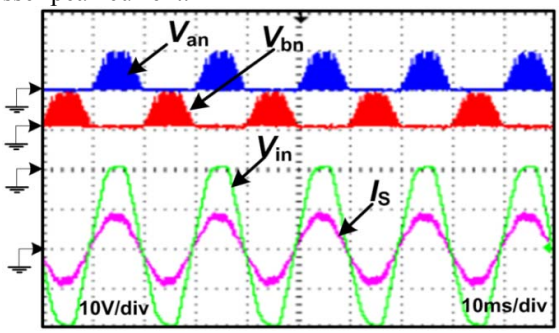
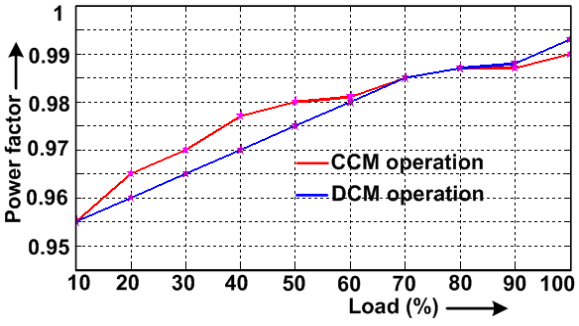
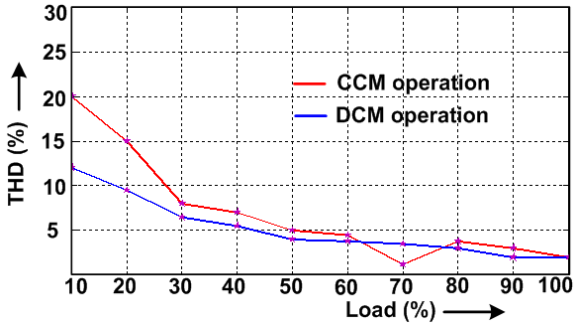


Fig. 8 Experimental result (a) source current approximately in phase with voltage



(a)



(b)

Fig. 9 Measured results (a) power factor versus change in load (b) THD versus change in load.

It can be seen from Fig. 10 that the efficiency under both CCM and DCM operations is lower at light load conditions (10%) and it gradually increases towards the load profile. In SBBR, the ripple component of inductor current is higher than the average component; therefore the RMS current is always higher in DCM mode, hence the efficiency of CCM is always slightly higher than DCM. The efficiency of SBBR is calculated by considering total losses occurring in the converter. In practical scenario the losses are estimated by various loss breakdowns in the SBBR converter has been taken into account. The total losses (PL_{total}) of SBBR converter can be estimated as below.

$$PL_{total} = P_{SW1} + P_{SW2} + P_{condS1} + P_{condS2} + P_{D1} + P_{D2} + P_{Dp} + P_{Dn} + P_L + P_C \quad (19)$$

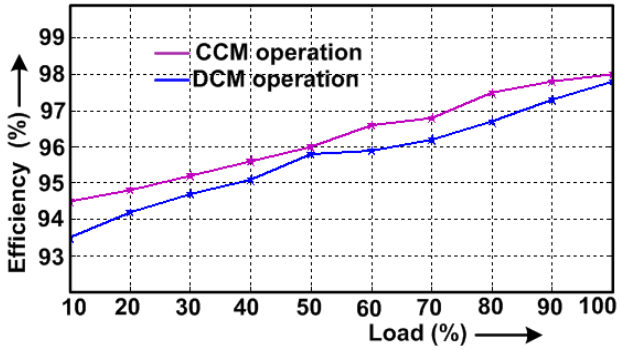


Fig. 10: The efficiency graph with variation of load.

where, P_{SW1} and P_{SW1} are switching losses of the switch S_1 and S_2 switches, respectively; P_{condS1} and P_{condS2} are the conduction losses of the S_1 and S_2 switches, respectively; P_{D1}, P_{D2}, P_{Dp} and P_{Dn} are the losses in diodes, PL and PC are inductor and capacitor losses, respectively. After observing all results of SBBR using CCM and DCM, the THD is better in DCM than CCM. However, the power factor and efficiency in DCM are lower than CCM. The picture of experimental setup is shown in Fig. 11. The power quality improvement has been tested and verified for SBBR in UPS application with CCM and DCM operation. The experimental results validated by using Spartan 3AN FPGA processor are identically matched with simulation results. Based on this study, the SBBR operates in stable region in both modes of operations. Experimental validation results show that DCM operation has better power factor and THD compared to CCM operation. However, the current stress increases and power handling capability reduces at heavy loads in DCM mode. The THD is above 5% in both DCM and CCM operations at light load conditions. Beyond 50% load, THD reduces to less than 5%

as per IEC 6100-3-2 standard. Moreover, the efficiency of SBBR in CCM operation is better than DCM. The complete control strategy of PFC is implemented in FPGA digital processor to increase accuracy.

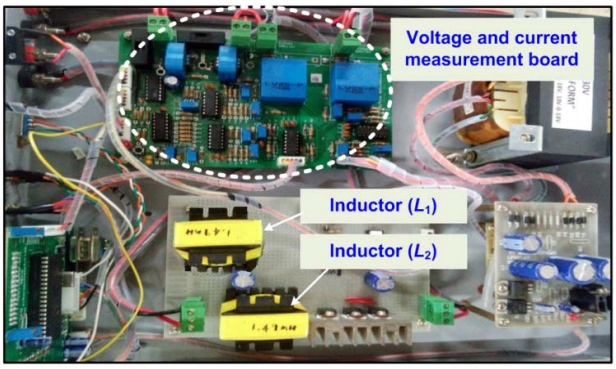


Fig. 11 Experimental set up picture

V. Conclusion

The power quality improvement has been tested and verified for SBBR in UPS application with CCM and DCM operation. The experimental results validated by using Spartan 3AN FPGA processor are identically matched with simulation results. Based on this study, the SBBR operates in stable region in both modes of operations. Experimental results show that DCM operation has better power factor and THD compared to CCM operation. However, the current stress increases and power handling capability reduces at heavy loads in DCM mode. The THD is above 5% in both DCM and CCM operations at light load conditions. Beyond 50% load, THD reduces to less than 5% as per IEC 6100-3-2 standard. Moreover, the efficiency of SBBR in CCM operation is better than DCM. The complete control strategy of PFC is implemented in FPGA digital processor to increase accuracy.

References

[1] Yeh, CC, and Manjrekar, MD. A reconfigurable uninterruptible power supply system for multiple power quality applications, *IEEE Transactions on Power Electronics*, 2007, 22, 1361-1372.

[2] S. Shan and L. Umanand, "A Unified Controller for Utility Interactive Uninterruptible Power Converters for Grid Connected and Autonomous Operations," *IEEE Transactions on Power Electronics*, July 2018. doi: 10.1109/TPEL.2018.2853636.

[3] Onar, OC, Kobayashi, J, Erb, DC, and Khaligh, A. A bidirectional high-power-quality grid interface with a novel bidirectional noninverted buck–boost converter for PHEVs, *IEEE Transactions onVehicular Technology*, 2012; 61:2018-2032.

[4] Zhou, G, Xu, J, Jin, Y. Improved digital peak current predictive control for switching DC–DC converters, *IET Power Electron*., 2011; 4:227–234.

[5] Sun, K, Zhang, L, Xing, Y, and Guerrero, JM. A distributed control strategy based on DC bus signaling for modular photovoltaic generation systems with battery energy storage, *IEEE Transactions on Power Electronics*, 2011; 26: 3032-3045.

[6] Su, B, Zhang, J, and Lu, Z.Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM, *IEEE Transactions on Power Electronics*, 2011; 26:427-435.

[7] De Bastiani Lange, A, Soeiro, TB., SilveiraOrtmann, M. and Lobo Heldwein, M. Three-Level Single-Phase Bridgeless PFC Rectifiers, *IEEE Transactions on Power Electronics*, 2015; 30: 2935-2949.

[8] Sayed, KF, Nakaoka, M, Morimoto, K, Kwon, SK. New high-frequency linked half-bridge soft switching PWM DC-DC converter with input DC rail side active edge resonant snubbers, *IET Power Electron*., 2010; 3:774–783.

[9] Foroozeshfar, R, Adib, E. New three phase discontinuous voltage mode cuk power factor correction converter for low power applications, *IET Power Electron*., 2013; 6: 946–953.

[10] Kim, YS., Sung, WY and Lee, BK.Comparative performance analysis of high density and efficiency PFC topologies, *IEEE Transactions on Power Electronics*, 2014; 29: 2666-2679.

[11] Sabzehgar, R, Moallem, M.Modelling and control of a boost converter for irregular input sources, *IET Power Electron*., 2012; 5: 702–709.

[12] Musavi, F, Eberle, W, and Dunford, WG.A phase shifted semi-bridgeless boost power factor corrected converter for plug in hybrid electric vehicle battery chargers. *In: Proc. IEEE Appl. Power Electron. Conf. Expo*.; 2011: 821–828.

[13] C. Lumbreras, J. M. Guerrero, D. Fernandez, D. Diaz, C. Gonzalez and F. Briz, "Analysis and Control of the Inductorless Boost Rectifier for Small Power Wind Energy Converters," *IEEE Transactions on Industry Applications*, Sept. 2018.doi: 10.1109/TIA.2018.2869099.

[14] Ou, SY, Tang, CY, and Chen, ZJ. Design and implementation of a ZCS-PWM half-bridge boost rectifier with output voltage balance control, *IEEE Transactions on Industrial Electronics*, 2012; 59: 46-56.

[15] M. B. Lakshmi, R. Thangasankaran, J. Gnanavadivel and S. T. J. Christa, "Performance Evaluation of Fuzzy Controlled Single Phase PWM Rectifier," 2018 Second International Conference on Electronics, Communication and Aerospace Technology (ICECA), COIMBATORE, India, 2018, pp. 1974-1979.

[16] Chan, C.Y.: Analysis and experimental investigation of a current controller for a full-bridge boost rectifier, *IET Power Electron*., 2013; 6: 270–275.

[17] S. Li, W. Qi, J. Wu, S. C. Tan and R. Hui, "Minimum Active Switch Requirements for Single-Phase PFC Rectifiers Without Electrolytic Capacitors," *IEEE Transactions on Power Electronics*, Spt. 2018. doi: 10.1109/TPEL.2018.2868872.

[18] Musavi, F, Eberle, W, and Dunford, WG.A phase-shifted gating technique with simplified current sensing for the semi-bridgeless AC–DC converter, *IEEE Transactions on Vehicular Technology*, 2013:6241568-1576.

[19] A. N. Arvindan and S. P. Vela, "Investigation for Improved Power Quality in Hysteresis Current Controlled Three-Phase Four-Wire Vienna Rectifier Topologies," *4th International Conference on Electrical Energy Systems (ICEES)*, 2018, pp. 485-493. doi: 10.1109/ICEES.2018.8442406.

[20] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer, 2001.