Mohit D. Ganeriwala

Assistant Professor · Department of Electrical Engineering

Indian Institute of Technology Kanpur, India

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Research Interest

Multiscale-Atomistic,numerical and Compact Modeling; Electrical characterization; Neuromorphic Computing; Two-dimensional materials; Advanced nanoscale FETs

Professional Experience

Assistant Professor — *India*
Department of Electrical Engineering,Indian Institute of Technology Kanpur — *2025-present*

Postdoctoral Researcher — *Granada, Spain*
Department of Electronics and Computer Technology, University of Granada — *2022-2025*
Marie Skłodowska-Curie Actions (MSCA) - Fellow
Multiscale modeling and simulation of 2D materials based devices for neuromorphic computing

Principal Engineer — *Bengaluru, India*
Globalfoundries (https://www.globalfoundries.com/) — *2020-2022*
World Wide Compact Modeling and Characterization

Education

PhD, Electrical Engineering — *Gujarat, India*
Indian Institute of Technology Gandhinagar — *July 2015 - July 2020*
Thesis: Compact electrostatic and transport model for high mobility III-V channel GAA MOS
Advisor: Prof. Nihar Ranjan Mohapatra
CGPA : 9.3/10 *at IIT Gandhinagar*
CGPA : 10/10 *at IIT Kanpur*

MTech, Electrical Engineering — *Gujarat, India*
Indian Institute of Technology Gandhinagar — *July 2013 - July 2015*
Thesis: Analysis of gate leakage current in high-k metal gate MOS transistors
Advisor: Prof. Nihar Ranjan Mohapatra
CGPA : 9.9/10 (*Institute Gold Medal*)

BTech, Electronics and Communication — *Gujarat, India*
Institute of Technology, Nirma University — *August 2008 - August 2012*
CGPA : 9.17/10 (*Department Gold Medal*)

Grants & Fellowships

2022-2024	**Marie Skłodowska-Curie Actions (MSCA) - Postdoctoral Grant (PI)**, European Commission, *Modeling of Ionic and Electronic Transport in 2D Materials Toward Memristive Applications in Neuromorphic Computing (MIETMAN)*	*€160932.48*
2020	**International Travel Support Grant**, Science and Engineering Research Board (SERB), Department of Science and Technology (DST), Government of India	
2019	**Atlas Research Travel Grant**, Indian Institute of Technology Gandhinagar	

2016 **Japan Student Services Organization (JASSO) Grant** , for research internship at Japan Advance Institute of Science and Technology (JAIST), Japan

2015 **Visvesvaraya PhD Fellowship**, Ministry of Electronics and Information Technology (MeitY), Government of India

Awards

2024 **Best Poster Award**, 8th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference

2022 **Best Poster Award**, 6th International Conference on Emerging Electronics (ICEE)

2020 **Outstanding Graduate Teaching Fellow**, Independent instructor for Post-Graduate course "Physics of Transistor", Indian Institute of Technology Gandhinagar

2019 **Best Paper Award (silver leaf)**, IEEE International Conference on Modeling of Systems Circuits and Devices (MOS-AK India 2019)

2018 **Best Manuscript** , 4th International Conference on Emerging Electronics (ICEE)

2015 **Institute Gold Medal (Academic excellence)**, Indian Institute of Technology Gandhinagar
Outstanding Research Award, Indian Institute of Technology Gandhinagar

2013, 2014 **Winner, Texas Instruments Analog Design Contest**, Indian Institute of Technology Gandhinagar

2012 **Department Gold Medal (Academic excellence)**, Indian of Technology, Nirma University
Best Project Award (final year BTech Project), Indian of Technology, Nirma University

Publications

Journal

Cruces, Sofia, **Mohit D. Ganeriwala**, Jimin Lee, Ke Ran, Janghyun Jo, Lukas Völkel, Dennis Braun et al. "Volatile and Nonvolatile Resistive Switching in Lateral 2D Molybdenum Disulfide-Based Memristive Devices" Nano Letters 25, no. 33 (2025): 12455-12462.

S. Cruces, **Mohit D. Ganeriwala**, J. Lee, L. Völkel, D. Braun, A. Grundmann, K. Ran, E. González Marín, H. Kalisch, M. Heuken, A. Vescan, J. Mayer, A. Godoy, A. Daus, and M. C. Lemme. "Volatile MoS2 Memristors with Lateral Silver Ion Migration for Artificial Neuron Applications", Small Sci., 5: 2400523, (2024).

Mohit D. Ganeriwala, Daniel Luque-Jarava, Francisco Pasadas, Juan J. Palacios, Francisco G. Ruiz, Andres Godoy, and Enrique G. Marin. "Effect of grain boundaries on metal atom migration and electronic transport in 2D TMD-based resistive switches." Nanoscale (2025).

Aishwarya Singh, **Mohit D. Ganeriwala**, Radhika Joglekar, and Nihar R. Mohapatra. "A Scalable Physics-Based Compact Model for Terminal Charge, Intrinsic Capacitance and Drain Current in Nanosheet Field Effect Transistors." IEEE Journal of the Electron Devices Society (2025).

Prabhat Khedgarkar, **M. D. Ganeriwala**, and Pardeep Duhan. "Investigation of the origin of 1/f noise in advanced 22 nm FDSOI MOSFETs", Appl. Phys. Lett. 2024, 125 (20), 203506.

M. D. Ganeriwala, Alejandro Toral-L´opez, Estela Calaforra-Ayuso, Francisco Pasadas, Francisco G. Ruiz, Enrique G. Marin, Andres Godoy. "Role of Point Defects and Ion Intercalation in Two-Dimensional Multilayer Transition Metal Dichalcogenide Memristors", ACS Applied Nano Materials 2024, 7 (21), 24857-24865.

J. Cuesta-Lopez, **M. D. Ganeriwala**, E. G. Marin, A. Toral-Lopez, F. Pasadas, F. G. Ruiz, A. Godoy; "Numerical study of synaptic behavior in amorphous HfO2-based ferroelectric-like FETs generated by voltage-driven ion migration". J. Appl. Phys. 2024, 136 (12), 124501.

M.D. Ganeriwala, R. Motos-Espada, E.G. Marin, Juan Cuesta-Lopez, M.G. Palomo, Noel Rodríguez, F. Ruiz and A. Godoy, "A flexible laser induced graphene memristor with volatile switching for neuromorphic applications" ACS Applied Materials & Interfaces 2024, 16 (37), 49724-49732

Toral-Lopez, A., E. G. Marin, F. Pasadas, **M. D. Ganeriwala**, F. G. Ruiz, D. Jiménez, and A. Godoy. "Reconfigurable frequency multipliers based on graphene field-effect transistors." Discover Nano 2023, 18 (1), 123.

M. D. Ganeriwala, Aishwarya Singh, Abhilash Dubey, Ramandeep Kaur, and Nihar R. Mohapatra. "A bottom-up scalable compact model for quantum confined nanosheet FETs." EEE Transactions on Electron Devices 2021, 69 (1), 380- 387.

M. D. Ganeriwala, Francisco G. Ruiz, Enrique G. Marin, and Nihar R. Mohapatra. "A unified compact model for electrostatics of III–V GAA transistors with different geometries." Journal of Computational Electronics 2021, 20 (5), 1676-1684.

Abdul Ghaffar, **M. D. Ganeriwala**, Kenta Hongo, Ryo Maezono, and Nihar R. Mohapatra. "Insights into the Mechanical and Electrical Properties of a Metal–Phosphorene Interface: An Ab Initio Study with a Wide Range of Metals." ACS omega 2021, 6 (11), 7795-7803.

M. D. Ganeriwala, Francisco G. Ruiz, Enrique G. Marin, Nihar R. Mohapatra, "A Compact model for III-V Nanowire electrostatics including band non-parabolicty", Journal of Computational Electronics 2019, 18 (4), 1229.

M. D. Ganeriwala, Francisco G. Ruiz, Enrique G. Marin, Nihar R. Mohapatra, "A Compact Charge and Surface Potential Model for III-V Cylindrical Nanowire Transistors", IEEE Transactions on Electro Devices 2019, 66 (1), 73.

M. D. Ganeriwala, Chandan Yadav, Francisco G Ruiz, Enrique G Marin and Nihar R. Mohapatra, "Modeling of Quantum Confinement and Capacitance in III-V Gate All Around 1D Transistors", IEEE Transactions on Electron Devices 2017, 64 (12), 4889.

Chandan Yadav, **M. D. Ganeriwala**, Nihar R. Mohapatra, Amit Agarwal and Yogesh Singh Chauhan, "Compact Modeling of Gate Capacitance in III-V Channel Quadruple-Gate FETs", IEEE Transactions on Nanotechnology 2017, 16 (4), 703.

M. D. Ganeriwala, Chandan Yadav, Nihar R. Mohapatra, Sourabh Khandelwal, Chenming Hu and Yogesh Singh Chauhan, "Modeling of charge and quantum capacitance in low effective mass III-V MOSFETs", Journal of Electron Devices Society 2016, 4 (6), 396.

Nihar R. Mohapatra, **M. D. Ganeriwala** and Satya Siva Naresh, "Effect of pre-gate carbon implant on narrow width behaviour and performance of High-K metal gate nMOS transistors", IEEE Transactions on Electron Devices 2016, 63 (7), 2708.

Pardeep Duhan, **M. D. Ganeriwala**, V. Ramgopal Rao and Nihar R. Mohapatra, "Anomalous Width Dependence of Gate Current in High-K Metal Gate NMOS Transistors", IEEE Electron Device Letters 2015, 36 (8), 739.

In Review

D. Braun, **M.D. Ganeriwala**, L. Völkel, K. Ran, S. Lukas, E.G. Marín, O. Hartwig, M. Prechtl, T. Wahlbrink, J. Mayer, G. S. Duesberg et. al., "Non-Volatile Resistive Switching of Polymer Residues in 2D Material Memristors" *(Nature Electronics)* arXiv preprint arXiv:2309.13900

Conferences

Aishwarya Singh, **M. D. Ganeriwala** and N. R. Mohapatra, "Physics-based Scalable Compact Model for Terminal Charge, Intrinsic Capacitance and Drain Current in Nanosheet FETs," 2024 8th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Bangalore, India, 2024, pp. 1-3. (Best Poster Presentation Award)

J. Cuesta-Lopez, E.G. Marin, M.C. Pardo, A. Medina-Rull, A. Toral-Lopez, **M.D. Ganeriwala**, F. Pasadas, F.G. Ruiz and A. Godoy, "MoS2-based ferroelectric-like memristive devices", 2-6 April 2023, Austria.

J. Cuesta-Lopez, E.G. Marin, A.Toral-Lopez, **M.D. Ganeriwala**, F.g. Ruiz, F. Pasadas and A. Godoy, "Volatile modulation of oxygen vacancy-related dipoles in gate insulators as a mechanism for non-volatile memories", 14th Spanish Conference on Electron Devices (CDE), 6-8 June 2023, Spain

M. C. Fernandez-Sanchez, M. Garcia-Palomo, **M. D. Ganeriwala**, R. Motos, A. Medina-Rull, F. Pasadas, E.G. Marin, A. Godoy and F. G. Ruiz, "Neuromorphic and logic circuit simulation using in-house fabricated GrAphene-based MEmristor (GAME)", 14th Spanish Conference on Electron Devices (CDE), 6-8 June 2023, Spain

Aishwarya Singh, **M. D. Ganeriwala**, Ramandeep Kaur, and Nihar R. Mohapatra. "A simplified approach to include confinement induced band structure changes into the NsFET compact model." In 2022 IEEE International Conference on Emerging Electronics (ICEE), pp. 1-5. IEEE, 2022. (Best Poster Presentation Award)

M. D. Ganeriwala, Francisco G. Ruiz, Enrique G. Marin, Nihar R. Mohapatra, "Significance of L-valley charges and a method to include it in electrostatic model of III-V GAA FETs", IEEE Electron Device Technology and Manufacturing (EDTM) Conference, Penang, Malaysia, March 15-18, 2020.

Sarathchandran GM, **M. D. Ganeriwala** and Nihar R. Mohapatra, "Capacitance and surface potential model for III-V Double-Gate MOSFETs", International Symposium on Devices, Circuits and Systems (ISDCS), Hiroshima, Japan, March 6-8, 2019.

M. D. Ganeriwala, Enrique G. Marin, Francisco G. Ruiz and Nihar R. Mohapatra, "A compact charge and surface potential model for III-V Quadruple-Gate with square geometry", 2019 IEEE International Conference on Modeling of Systems Circuits and Devices (MOS-AK India 2019), Hyderabad, India, February 25-27, 2019. (Best Paper Award, Silver Leaf).

Amratansh Gupta, **M. D. Ganeriwala** and Nihar R. Mohapatra, "A unified charge centroid model for silicon and low effective mass III-V channel double gate MOS Transistors", 32nd International Conference on VLSI Design (VLSID), Delhi, India, January 4-8, 2019.

M. D. Ganeriwala, Sarathchandran GM., Nihar R. Mohapatra, "A simple charge and capacitance compact model for asymmetric III-V DGFETs using CCDA", IEEE International Conference on Emerging Electronics (ICEE), Bangalore, India, December 16-19, 2018. (Best Manuscript Award).

M. D. Ganeriwala, Enrique G. Marin, Francisco G. Ruiz and Nihar R. Mohapatra, "Computationally efficient analytic charge model for III-V cylindrical nanowire transistors", Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2018 (EUROSOI-ULIS), Granada, Spain, March 2018.

M. D. Ganeriwala, Pardeep Duhan and Nihar R. Mohapatra, "Detailed analysis of carrier transport through multi-stack gate dielectrics of modern MOS transistors", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, December 27-30, 2016.

Research Stays & Internships

May 16 - Aug 16	**Japan Advance Institute of Sceience and Technology (JAIST)**, *Prof. Ryo Maezono, Materials simulations using ab-initio methods*	*Japan*
July 15 - April 16	**Indian Institute of Technology Kanpur**, *Nano Lab, Prof. Yogesh Chauhan, Compact modeling of III-V double gate transistors*	*India*
Jan 12 - May 12	**Space Application Centre, Indian Space Research Organization (SAC-ISRO)**, *Verilog-A implementation of Viterbi decoder*	*India*

Invited Talks & Workshops

2025	The Role of Point and Extended Defects in 2D-Materials Based Memristors for Neuromorphic Computing: An Atomistic Study, *Workshop, ESSERC 2025, Munich*	*Germany*
2025	An Atomistic Study of Point and Extended Defect in Performance of 2D Materials based Memristors for Neuromorphic Computing, *IHT, University of Stuttgart*	*Germany*
2025	The role of point and extended defects in 2D-materials based memristor for neuromorphic computing: An atomistic study, *The chair of ELD, RWTH University Aachen*	*Germany*
2023	2D Materials based Memristors : A DFT Study, *AtomElix group, Universidad Autónoma de Madrid*	*Spain*
2023	2D Materials Based Memristors for Neuromorphic Computing, *The Group of Computer Architecture (AGRA), University of Bremen*	*Germany*
2018	Modeling of Quantum Confinement of Capacitance in III-V Gate All around 1-D Transistors, *Integrated Quantum Devices Area, Division of Electrical, Electronics and Information Engineering, Osaka University*	*Japan*
2018	Development and Testing of Advanced Physical Models for III-V Cylindrical Nanowire Transistors, *Department of Electronics and Computer Technology, University of Granada*	*Spain*

Teaching Experience

Post Graduate Course

Spring 23	**Nanoelectronics**, University of Granada, Spain Seminars and Special Sessions
Fall 20	**EE 644 Physics of Transistors**, Indian Institute of Technology Gandhinagar, India Independent Instructor, *Review Score: 3.86/4* , *(Best GTF Award)*
Fall 19	**EE 644 Physics of Transistors**, Indian Institute of Technology Gandhinagar, India Co-Instructor, *Review Score: 3.78/4*
Spring 19	**EE 614 Special Topics in Electrical Engineering (MOS Transistor Modeling)**, Indian Institute of Technology Gandhinagar, India Co-Instructor

Under Graduate Course

Fall 22	**Circuit Analysis**, University of Granada, Spain, Lab Tutor
Spring 19,18	**ES 104 Analog and Digital Electronics**, Indian Institute of Technology Gandhinagar, India Independent Tutor, Review Score: 3.78/4

Mentoring

As Co-guide

2022-2023	Julián Guerrero Cánovas, Bsc Physics, Study of ion transport in batteries using Q-ATK	*UGR*
2021-2022	Estela Calaforra Ayuso, Msc Physics, Study of defects in 2-dimensional TMDs : A DFT study	*UGR*
2024-2025	David Alarcos Teruel, BTech, Fabrication and advanced characterization of graphene-based memristive devices	*UGR*

As Student Mentor (IIT Gandhinagar)

PhD Student	Aishwarya Singh , Circuit simulation based performance benchmarking of 2D FETs, *Independent study project*
MTech/Msc Students	Sarath Chandran GM, Modeling of III-V channel double-gate MOS transistors, *Master Thesis* C.Yashwanth Sai Kiran, Contact resistance optimisation in HEMT, *Master Thesis* Abdul Ghaffar and Sujoy Saha, DFT based investigation of black phosphorous-metal contact properties, *Msc Thesis*
Interns	Amratansh Gupta, Charge centroid model in III-V channel multi-gate transistors Rohan Sengupta Numerical simulations of III-V channel double-gate MOS transistors Biswajeet Sahoo Python based interactive tool for simulation of the MOS electrostatics

Service & Outreach

Outreach

2023	Semana de la Ciencia, Science outreach for high school students
2023	European Researchers Night, Science outreach for General Public
2022	European Researchers Night, Science outreach for General Public

Technical Programm Committee

2024	8th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2024, Track : Modeling and Simulations

Reviewer

Journal	IEEE - Transactions on Electron Devices (TED), Electron Device Letter (EDL), Journal of Electron device Society (JEDS), Elsevier - Microelectronic Engineering, Solid-State Electronics, ACS - NanoLetter, Applied Material and Interfaces, Applied Nano Materials , Springer - Nano Micro Letter,
Conference	IEEE Electron Devices Technology and Manufacturing (EDTM), 2024 International Workshop on Physics of Semiconductor Devices (IWPSD), 2023 IEEE India Council International Conference (INDICON), 2019

Administrative

2016-2019	Lab/System administrator nanoDC lab, IIT Gandhinagar
2014-2015	Vice Chairperson, IEEE Student Section, IIT Gandhinagar