SIDBI INNOVATION AND INCUBATION CENTRE
INDIAN INSTITUTE OF TECHNOLOGY KANPUR

To,

Ref No: IIT/ SIIC/Mole/FPGA Board/BV/19-11-2014

INVITATION FOR QUOTATIONS FOR SUPPLY OF FPGA DEVELOPMENT BOARD

Brief Description of the Goods	Specifications*	Qty.	Delivery Period	Place of Delivery	Installation Requirement if any
FPGA DEVELOPMENT BOARD	Mentioned below	05	20 Days	Central Store, IIT Kanpur	Yes

FPGA Development Board

The Cyclone V GT FPGA Development Kit features the following:

- Cyclone V GT FPGA development board
  - Featured devices
    - Cyclone V GT FPGA—5CGTFD9E5F35C7N
    - MAX® V CPLD—5M2210ZF256 (System Controller)
    - MAX II CPLD—EPM570GT100C3N (On-Board USB Blaster™ II)
    - MAX II CPLD—EPM570ZM100 (ASSP CPLD footprint)
  - Configuration
    - Embedded USB-Blaster II (JTAG)
    - Fast Passive Parallel (PFL)
    - Altera EPCQ—EPCQ256SI16N (Quad Serial Configuration Device)
  - Memory devices
    - 384 MB x40 hard memory controller (HMC) DDR3 SDRAM with error correction code (ECC)
    - 512 MB x64 soft memory controller (SMC) DDR3 SDRAM
    - 1 Gb x16 sync flash
  - Standard communication ports
    - PCIe x4 edge connector
    - Gigabit Ethernet (GbE)
    - One SMA clock output
    - Two universal high-speed mezzanine card (HSMC) connectors, each with four high-speed serial transciever channels
    - One serial digital interface (SDI) channel —1 SMB for RX and 1 SMB for TX
      - Channel shared with HSMA via resistor stuffing option
  - Push buttons, DIP switches, and LEDs
  - Clocking
    - Programmable clock generator for FPGA reference clock input
    - 125 MHz LVDS oscillator for FPGA reference clock input
    - 148.5/148.35 MHz LVDS VCXO for FPGA reference clock input
    - 50 MHz single-ended oscillator for FPGA and MAXV CPLD clock input

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- 100 MHz single-ended oscillator for MAX V CPLD configuration clock input
- SMA input (LVPECL)

- Power
  - Laptop DC Input 14 – 20 V adapter
  - PCIe edge connector
- System monitoring circuit
  - Power (Voltage, Current, Wattage)
- Mechanical
  - PCIe card standard size (4.376" x 6.600")

- Cyclone V GT FPGA Development Kit software
  - Design examples
    - PCIe loop back and reference design
    - Board test system (BTS)*
    - Board update portal (BUP)*
      - Includes Nios® II embedded soft processor and Ethernet
    - Complete documentation
- Cyclone V GT FPGA Kit with Development Kit Edition (DKE) of the Quartus II software (Windows platform only).
- **Renowned Manufacturers like: TI**

Terms & Condition

1. **The scope includes:**
   a. Setting up machine in IIT Kanpur.
   b. Initial Installation and configuration.
   c. Training.

2. **Bid Price**

   a) The contract shall be for the full quantity as described above. Corrections, if any, shall be made by crossing out, initialing, dating and re writing.

   b) All duties, taxes and other levies payable on the raw materials and components shall be included in the total price. **Except Central Excise Duty & CDEC** (custom duty), as IIT Kanpur is exempted from these duty.

   c) Sales tax in connection with the sale shall be shown separately.

   d) The rates quoted by the bidder shall be fixed for the duration of the contract and shall not be subject to adjustment on any account.

   e) The Prices shall be quoted in Indian Rupees only.

3. Each bidder shall submit only one quotation.

4. **Validity of Quotation**

Quotation shall remain valid for a period not less than 60 days after the deadline date specified for submission.

5. **Evaluation of Quotations**

The Purchaser will evaluate and compare the quotations determined to be substantially responsive i.e. which

(a) are properly signed ; and

(b) Conform to the terms and conditions, and specification

The Quotations would be evaluated separately for each item

Sales tax in connection with sale of goods shall not be taken into account in evaluation.

6. **Award of contract**

The Purchaser will award the contract to the bidder whose quotation has been determined to be substantially responsive (includes technically suitable) and who has offered the lowest evaluated quotation price.

6.1 Notwithstanding the above, **the Purchaser reserves the right to accept or reject any quotations and to cancel the bidding process and reject all quotations at any time prior to the award of contract.**

6.2 The bidder whose bid is accepted will be notified of the award of contract by the Purchaser prior to expiration of the quotation validity period. The terms of the accepted offer shall be incorporated in the purchase order.

7. Payment shall be 90% against the delivery and 10% after satisfactory installation & configuration.

8. Warranty/ guarantee shall be 60 months to the supplied goods.

9. You are requested to provide your offer latest by 2.30 p.m. hours on 29/11/2014

10. We look forward to receiving your quotations and thank you for your interest in this project.

FORMAT OF QUOTATION

Sl. No.	Description Goods	Specifications	Qty.	Unit	Quoted Unit Rate in Rs.	Total Amount	
						In Figures	In Words
	TOTAL						
	Sales Tax						

Gross Total Cost : Rs. .....

We agree to supply the above goods in accordance with the technical specifications for a total contract price of Rs. .....(amount in figures) (Rs. ..... amount in words) within the period specified in the Invitation for Quotations.

We also confirm that the normal commercial warrantee/guarantee of 60 months shall apply to the offered goods.

Signature of Supplier

SPECIAL CONDITION

1) **Authorization from Manufacturer**

In the case of a Bidder offering to supply goods under the contract which the Bidder did not manufacture or otherwise produce, the Bidder has been duly authorized by the goods' Manufacturer or producer to supply the goods in India.

2) **Proof of Manufacturing and past performance.**

Details of experience and past performance of the bidder on equipment offered and on those of similar nature within the past one years and details of current contracts in hand and other commitments.

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