Experimental Implementation of new N-level Single-phase Multilevel Inverter

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Abstract— **Sinusoidal nature of inverter output voltage reduces the harmonic content thus enables the effective and efficient power conversion in various industrial drive applications. Multilevel inverter conquers the overall market over conventional inverters by an additional feature of non-filter requirement. Researchers are looking forward to minimize the overall components of the multilevel inverters. A new and novel inverter is projected in this paper with the least possible number of components mainly focuses to reduce the power switches thus to minimize the complexity, cost and space of the complete system. Proposed inverter is generalized in structure and can be used for same or different magnitudes of available DC sources. A 7-level as well as 13-level inverter is designed for the proposed topology and the real-time results verifies the simulation results thereby validates the feasibility of the inverter. Moreover, the proposed work is tallied with some newly invented topologies with reduced components.**

Keywords— Power-electronic switches, DC-AC converters, 7-Level/13-Level Inverter, Sinusoidal PWM.

I. INTRODUCTION

Numerous drawbacks such as higher distortion in the output voltage, higher switching stress are witnessed in classical or conventional two-level inverters [1]. However, the appearance of Multilevel inverter (MLI) offers several advantages such as low harmonic distortion [2,3], lower voltage stress, lower switching losses along with some of the eye-catching features like healthier electromagnetic compatibility, higher efficiency, applications in high voltage, high power [4]. The first configuration of MLI that capable to amalgamate higher output voltage levels for medium voltage applications was none other than Neutral point clamped (NPC) [5] among the three of classical topologies of MLIs. To overcome the drawbacks of increased number of clamping diodes in NPC-MLI, the Flying Capacitor (FC) MLI topology was introduced. Anyway, major drawback lies with FC-MLI about the capacitor voltage balancing technique [6]. However, demerits of aforesaid classical MLIs are overcome by the cascaded H-Bridge configuration that does not requires any surplus components like diodes and capacitors in the circuit with simple structure. It can be simply observed that with the symmetric CHB inverter i.e. with same value of the DC links, the number of power switches and DC sources rise with rise in the output voltage level [7] whereas asymmetrical CHB multilevel inverter consumes different value of DC links voltage having same number of overall components. Therefore, the need strikes to develop a MLI with reduced number of components and DC voltage sources for both symmetrical and the asymmetrical MLI.

The aim of the present researchers is to design and develop reduced switch MLI configurations having minimal number of IGBTs, gate drivers, DC voltage sources, TSV and losses. In this paper, 7-level inverter and 13-level inverter is developed and experimental results are well matched with the simulation results. Recent discovered topology of MLIs [8-13] are compared with the proposed one and it was found better among them. The MLI proposed in [8] is evolved from the existing source-based cross-connected multilevel inverter (CCS-MLI) for interfacing renewable energy sources with low/medium- and high voltage grids. The basic block and generalized structure of proposed MLI for HVA and L/M VA are presented. Proposed block (fundamental) includes 6 uni-directional and 1 bi-directional switch along with a voltage divider and 2 DC sources. The new structure configured in [9] produces all odd and even voltage levels under symmetric as well as in asymmetric mode of operation. Proposed structure in [9] comprises semi-half-bridge cells connected in series with criss-crossed power switches. In this paper two topologies are developed (9-level symmetrical and 15-level in asymmetrical) and another is extended topology (21 level in asymmetrical). In [10], a new MLI topology presented a new named Square T-Type (ST-Type) module that can generate 17 levels with reduced components that can be used in high voltage/power applications with unequal DC sources. A square T-type module produces 17 levels by 12 switches and 4 unequal DC sources. A nearest level control method as a switching technique is used to produce high quality output voltage with lower harmonic contents. Two novel compact modules were presented for CCM-MLI in [11]. The proposed 7LCM and 13LCM topologies not only realize a low number of conducting switch count for all voltage levels, but also guarantee smooth transition between voltage levels during dead-time. The letter in [12] proposed a basic cell i.e. 4-level symmetrical sub-module or a hybrid cascaded multilevel inverter (HCMLI) topology is formed by the combination of *n* sub-modules and a full-bridge. A two-stage switched-capacitor based multilevel inverter possesses a drawback such that switches in the second stage (i.e. H-bridge) endure higher voltage stress. To resolve this problem, this letter in [13] proposes a single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter which ensures the peak inverse voltage across all switches within the dc source voltage.

This paper is divided into some important sections such as working of the proposed topology in section-II, explaining the control algorithm in section-III, comparison with existed topology in section-IV, simulation and experimental results in section-V, conclusion in section-VI.

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II. PROPOSED TOPOLOGY

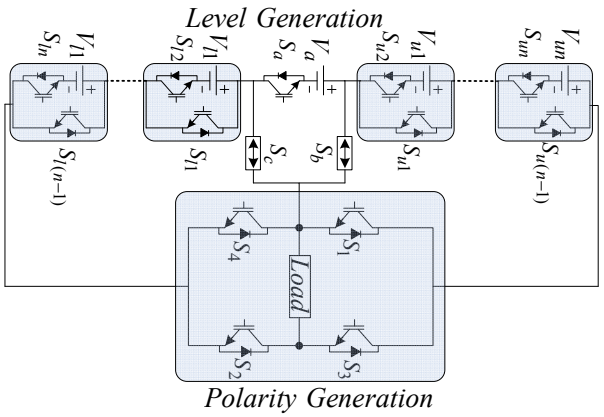


Fig. 1(a). Generalized structure of proposed topology.

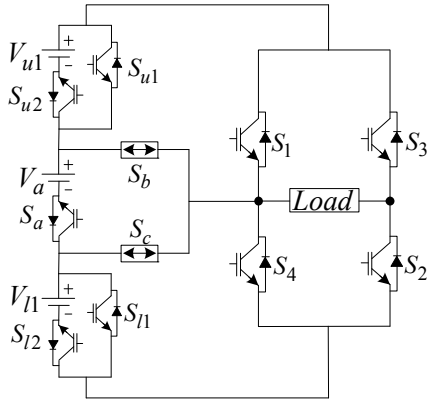


Fig. 1(b). Proposed topology with different voltage-levels

(i) 7-level ; $V_{l1}=V_a=V_{u1}=V_{dc}$ (ii) 9-level ; $V_{l1}=V_{dc}$, $V_a=V_{dc}$, $V_{u1}=2V_{dc}$
(iii) 11-level ; $V_{l1}=V_{dc}$, $V_a=2V_{dc}$, $V_{u1}=2V_{dc}$ (iv) 13-level ; $V_{l1}=V_{dc}$, $V_a=2V_{dc}$, $V_{u1}=3V_{dc}$
(v) 15-level ; $V_{l1}=V_{dc}$, $V_a=2V_{dc}$, $V_{u1}=4V_{dc}$

Generalized structure of proposed multilevel inverter topology as visualized in Fig. 1a can be segregated into two major parts i.e. level generating unit and polarity generating units. H-bridge is used in this topology for polarity generation whereas the level generation occurs in two parts i.e. upper and lower as indicated as faded block named 'Unit'. Each unit contains two switches and a DC source. Fig. 1b shows the proposed topology that can generate 7-level/9-level/11-level/13-level/15-level using different values of DC sources and this structure can be further extended by adding the aforementioned units in the upper as well as the lower portion in equal numbers. Thus, it can be said that if one unit is added on the upper portion of the basic structure, one unit would be added in the lower portion as well. The power switches in each units in the upper portion are named as S_{u1}, S_{u2}; S_{u3}, S_{u4} ;.....; $S_{u(n\text{-}1)}$, S_{un} in unit-1, unit-2 and unit-*n* respectively. Similarly, the power switches in each units in the lower portion are in unit-1, unit-2 and unit-*n* are named as S_{l1}, S_{l2}, S_{l3}, S_{l4};.....;$S_{l(n\text{-}1)}$, S_{ln} respectively. The magnitude of the DC sources is set according to the requirement of the voltage levels or voltage steps. The beauty of the proposed MLI structure confirms its operation for binary ratio of DC voltage magnitude i.e. $1{:}2{:}4{:}8{:}...2^{Ndc\text{-}1}{:}2^{Ndc}$ where N_{dc} denotes number of DC sources. Say, for the available basic structure and considering the DC voltage magnitude in the ratio 1:2:4:8, three DC sources V_{l1}, V_a and V_{u1} will have magnitudes as V_{dc}, $2V_{dc}$, $4V_{dc}$ respectively. If one unit is further extended in each portion i.e. one unit in upper as well as one unit in lower portion, 5 DC sources V_{l2}, V_{l1}, V_a, V_{u1} and V_{u2} will have magnitudes as V_{dc}, $2V_{dc}$, $4V_{dc}$, $8V_{dc}$, $16V_{dc}$ respectively. Two of the total power switches S_b and S_c are bi-directional switches (one power switch with four anti-parallel diodes).

Proposed basic structure of the topology generates 7-level output for all same values DC magnitudes whereas 13-level output is obtained for all different value of DC magnitudes extending one unit in upper portion and one unit in the lower portion as well.

III. MODES OF OPERATION

Among some of the renowned control strategies used for multilevel inverter such as nearest level modulation [14], SHE (selective harmonic elimination) [15], sine based carrier PWM [16][17], phase-shifted modulation [18], carrier based sine PWM is opted for the proposed topology for being simpler and ease of control. The switching frequency of the power switches f_{sw} is considered to be 3 kHz. dSPACE-1103 is used for the generation of real-time pulses for implementation in prototype model. Six triangular carriers are kept on upon another thus also called level-shifted PWM (Pulse width Modulation).

Table. 1. Switching table of proposed 7-Level MLI for symmetrical DC sources ($V_{u1}=V_{l1}=V_a=V_{dc}$)

Conducting switches status 1=ON; 0= OFF											Modes
S_{u1}	S_{u2}	S_a	S_b	S_c	S_{l1}	S_{l2}	S_1	S_2	S_3	S_4	
0	1	1	0	0	0	1	1	1	0	0	M-1
0	1	1	0	1	0	0	0	0	1	0	M-2
1	0	1	0	1	0	0	0	0	1	0	M-3
0	0	0	0	1	0	1	0	1	0	0	M-4
0	0	0	0	1	1	0	0	1	0	0	M-5
0	0	1	1	0	1	0	0	1	0	0	M-6
0	1	1	0	0	0	1	0	0	1	1	M-7

Further, all these triangular carriers can be arranged in different fashion i.e. PD (Phase disposition), POD (Phase opposition disposition) and APOD (Alternate Phase opposition disposition) [16]. Moreover, these aforementioned types of PWM can be of fixed frequency or varied frequency i.e. all the triangular carriers can be of fixed frequency or all the triangular carriers could be of different frequency.

The working logic behind all the techniques lies about the comparison of sinusoidal signal or the reference signal with the carrier signals. After generating the signals, the decoder plays an important role that helps to create the appropriate switching for the respective power switches. In this paper, LS-PWM (Level-shifted Pulse width Modulation) is employed for fixed frequency based PD method. The switching pattern derived from simulation as well as real-time of the respective switches are well depicted in Fig. 2(a) and Fig. 2(b) respectively for one cycle of reference signal (sinusoidal signal). All the modes i.e. steps realizing the generation of various voltage steps or voltage levels are depicted as pictorial presentation in Fig. 3, where the darken line shows the voltage generation path of the proposed topology for 7-level inverter (symmetrical in structure). The

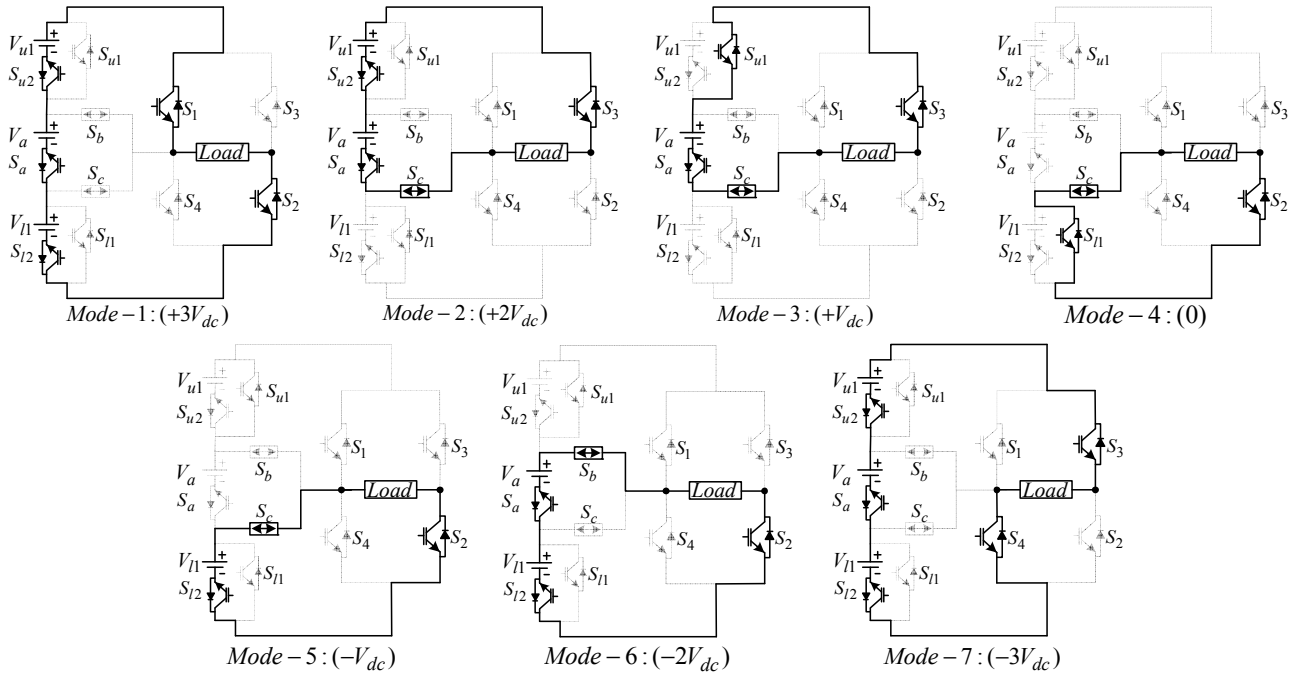


Fig. 3. Modes of operation

steps with magnitude of output voltage are well mentioned in theoretical explanation whereas the switching sequence of the power switches are indicated as 1=ON and 0=OFF in Table 1. Various modes depicting the generation of different voltage levels are explained as below.

- To obtain $+3V_{dc}$, power switches S_{u2}, S_a, S_{l2}, S_1, S_2 are made ON with the remaining switches are kept OFF to generate +114 V in output.
- $+2V_{dc}$ is obtained when power switches S_{u2}, S_a, S_c, S_3 are kept ON with the remaining power switches are switched OFF to generate +76 V in output.
- $+V_{dc}$ is obtained when power switches S_{u1}, S_a, S_c, S_3 are kept ON with the remaining power switches are switched OFF to generate +38 V in output.

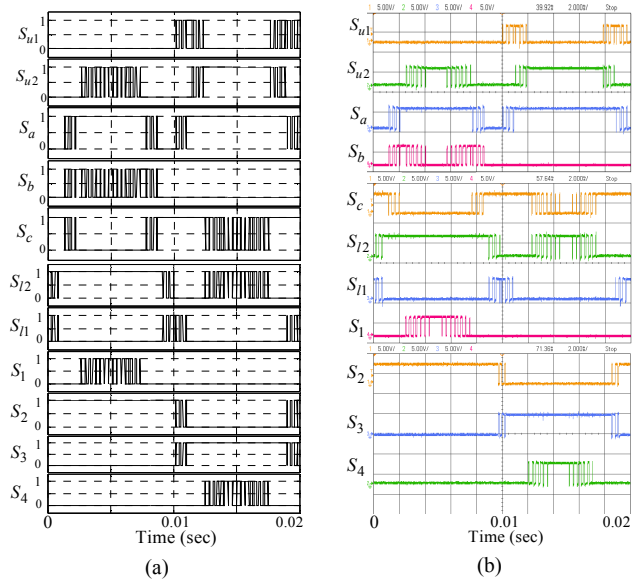


Fig. 2. Switching pulses of the power switches
(a) Simulation Results.
(b) Experimental Results.

- Zero Voltage is obtained when power switches S_{l2}, S_c, S_{23} are kept ON with the remaining power switches are switched OFF to generate 0V in output.
- $-V_{dc}$ is obtained when power switches S_{l1}, S_2, S_c are kept ON with the remaining power switches are switched OFF to generate -38V in output.
- To obtain $-2V_{dc}$, power switches S_{l1}, S_a, S_b, S_2 are kept ON with the remaining power switches are switched OFF to generate -76V in output.
- $-3V_{dc}$ is obtained when power switches S_{u2}, S_a, S_{u2}, S_4, S_3 are kept ON with the remaining power switches are switched OFF to generate -114V in output.

IV. Comparison with New Topologies

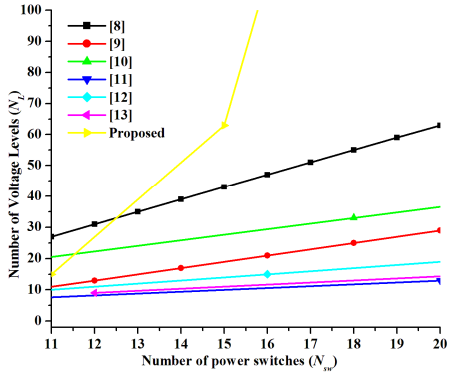
There are various topologies of MLI rather than classical MLI topologies that have been seeking attention throughout the globe for their economic cost, simpler circuit, ease in control, less maintainenece, less space requirement. The proposed topology is compared with some of the well-established topology recently suggested by various researchers studied in [8-13]. The generalized formulae for all the required components i.e. total number of power switches (N_{sw}), DC sources (N_{dc}), uni-directional switches (N_U), bi-directional switches (N_B) of the proposed topology are compared with aforesaid parameters of newly proposed topologies studied in [8-13] has been listed in Table 2.

Table. 2. Comparison of all components of the proposed MLI topology (1:2:4:8) and other recently proposed MLIs.

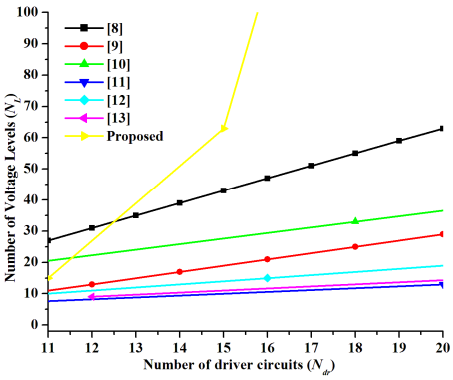
Types of MLI	Components count			
	(N_L)	(N_B)	(N_U)	(N_{dc})
[8]	($4N_{sw}$-17)	N_{sw}-6	6	N_{sw}-3
[9]	($2N_{sw}$-11)	NA	N_{sw}	N_{sw}-6
[10]	($16N_{sw}$+9)/9	N_{sw}/3	$2N_{sw}$/3	$4N_{sw}$/9
[11]	($3N_{sw}$+4)/4	NA	N_{sw}	$3N_{sw}$/8
[12]	(N_{sw}-1)	NA	N_{sw}	(N_{sw}-2)/2
[13]	($2N_{sw}$+3)/3	NA	N_{sw}	N_{sw}/4
Proposed	[$4^{(Nsw-3)/4}$-1]	2	N_{sw}-2	(N_{sw}-5)/2

The remarkable point of the proposed topology lies with the point that all the comparison of the required components are done considering the binary voltage ratio (1:2:4:8...2^{Ndc}) for the available DC sources.

Moreover, the graph is incorporated showing the plot between number of voltage levels (N_L) versus number of power switches (N_{sw}) and number of voltage levels (N_L) versus number of driver circuits (N_{dr}) in Fig. 4a and 4b respectively.



(a)

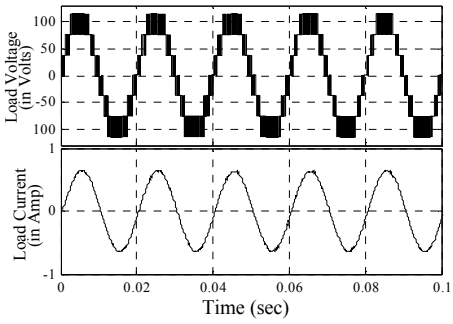


(b)

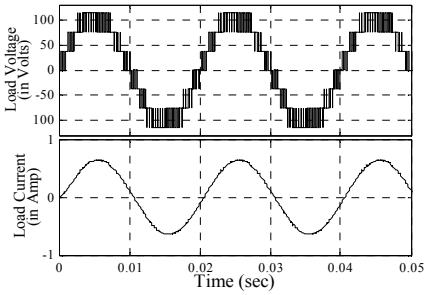
Fig. 4. Comparison b/w proposed MLI and other existed MLIs.
(a) N_{sw} versus N_L. (b) N_{sw} versus N_{dr}.

It can be noticed that reducing the number of power switches reduces the driver circuit but allows the overall circuit for less maintainenece, easier to implement, easier detection of fault, lower cost, less complex, less required space.

V. SIMULATION AND EXPERIMENTAL RESULTS



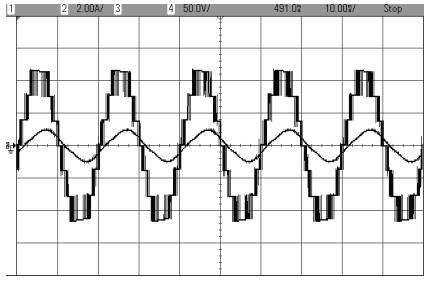
(a)



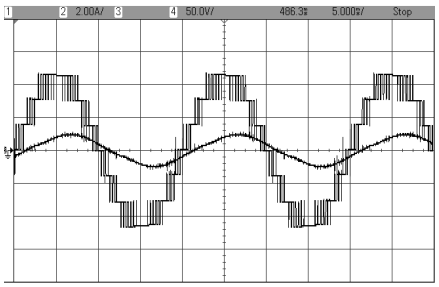
(b)

Fig. 5. Simulation Results of 7-level
(a) Load Voltage and current (5-Cycles).
(b) Load Voltage and current (2.5-Cycles).

A 7-Level inverter (symmetric value of DC sources) is designed and tested in MATLAB having same magnitude of DC sources say 38V i.e. $V_{ul}=V_{l1}=V_a=V_{dc}=38$V. So, the maximum peak of output voltage is +114V and minimum peak of output voltage -114V. The test is carried out with RL-Load where R=170Ω, L=100mH is chosen. To avoid confusion in vision of 5-cycles, further output results (load voltage & load current) is provided for 2.5-cycles as depicted in Fig. 5a & 5b respectively.



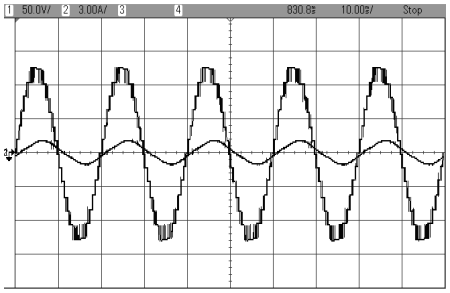
(a)



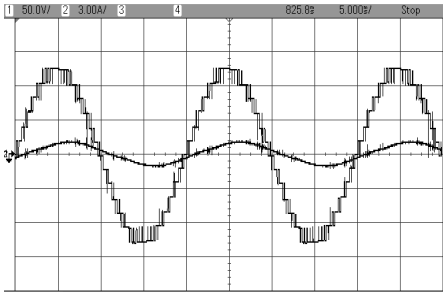
(b)

Fig. 6. Experimental Results of 7-level
(a) Load Voltage and current (5-Cycles).
(b) Load Voltage and current (2.5-Cycles).

An experimental set-up is also designed for the same i.e. 7-level inverter (symmetrical) thus verifying the smoother working of the proposed topology. The simulation as well as the experimental results showing the output voltage with load current is added in this paper for the same parameter of load and magnitude of DC sources. It can be noticed that the experimental results follows the simulation results as depicted in Fig. 6a & 6b for 2.5-cycle and 5-cycle respectively.



(a)



(b)

Fig. 7. Experimental Results of 13-level
(a) Load Voltage and current (5-Cycles).
(b) Load Voltage and current (2.5-Cycles).

Nevertheless, a 13-level inverter is designed by choosing the magnitude of DC voltage in the ratio of 1:2:3 i.e. V_{ul}=21V, V_a=42V,V_{ll}=63V thereby generating +126V as the maximum peak of the output voltage and -126V as the minimum peak of the output voltage for R=170Ω, L=100mH. Fig. 7a & 7b shows the load voltage and current for 5-cycles and 2.5-cycles respectively. All the results (symmetrical & asymmetrical) is incorporated to proof the effectiveness of the proposed topology.

VI. Conclusion

This paper introduces a novel and generalized topology that can be extended by adding the units. A 7-level as well as 13-level inverter is simulated and the outcomes are experimentally verified with RL-Load. The topology serves better outcome or result in terms of required components. The generalized formulae is derived for the proposed topology as well as the existed MLI topology and was found better in terms of the economic cost, simpler circuit, ease in control, less maintainenece, less space requirement. Thus, the proposed reduced switch MLI is concluded to be better than newly suggested MLIs in [7-13].

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