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Subject: [acadstaff] K R Sarma and Dr. M. Ramamoorthy Distinguished Series Lecture by Prof. Saurabh Lodha on "Engineering the strain and neuromorphic performance of 2D-TMD transistors"
From: "Avinash Lahgere" <alahgere@iitk.ac.in>
Date: Fri, February 21, 2025 12:58 pm
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All interested are cordially invited to attend the following K R Sarma and Dr. M. Ramamoorthy Distinguished Series Lecture:

Title: "Engineering the strain and neuromorphic performance of 2D-TMD transistors"

Speaker: Prof. Saurabh Lodha, Indian Institute of Technology Bombay (IITB)

Date/Time: 25th February 2025, 10:30 AM IST

Venue: ACES - 214, EE Department

Abstract:

In recent years, researchers have leveraged the unique physical properties of layered two-dimensional (2D) van der Waals (vdW) materials, such as a wide range of thickness-dependent bandgaps and facile fabrication of heterostructures with defect-free heterointerfaces, for several electronic applications. At the same time, their optical and electrical properties can be controlled using strain tuning of band structure parameters because of their high tensile strength, as well as via electrostatic gating based tuning of carrier concentrations because of their ultra-thin nature.

This presentation will first describe recent results from our group on engineering the strain-modulated performance of transistors based on 2D vdW transition metal dichalcogenide (TMD) semiconductors. Specifically, an electrically actuated piezo-stack is shown to fine-tune optical and electrical parameters of MoS₂ field-effect transistors with tensile as well as compressive strain, offering improved control and integration possibilities over existing mechanical methods. [1] Next, we will describe the use of independent electrostatic gating of contact and channel barriers in 2D TMD transistors towards realizing neuronal spiking behaviour, closely mimicking biological neurons with functionalities such as spike- frequency adaptation and post-inhibitory rebound, at a low energy consumption of 3.5 pJ/spike. [2]

References

[1] A. Varghese, A. Pandey, P. Sharma, Y. Yin, N. Medhekar, S. Lodha, Nano letters, 24, 28, 8472-8480, 2024.

[2] K. Thakar, B. Rajendran, S. Lodha, npj 2D Materials and Applications, 7 (68), 2023.

Biography:

Prof. Saurabh Lodha is the P. K. Kelkar Chair Professor at the Department of Electrical Engineering, Indian Institute of Technology (IIT) Bombay in India. He graduated from IIT Bombay in 1999 with a B. Tech (EE) followed by a Masters (ECE) and PhD (ECE) from Purdue University, USA, in 2001 and 2004 respectively. From 2005-2010 he worked at Intel Corporation in Portland, USA, on the research and development of 45, 32 and 22 nm Si CMOS technologies. He joined IIT Bombay in 2010 where he is also the PI of the IITB-OSU Frontier Research Center. His research interests span devices and materials in the areas of advanced CMOS technologies, 2D (opto)electronics and gallium oxide power electronics. He has been awarded the Swarna Jayanti fellowship (2017) and the Young Career Award (2020) by the Department of Science and Technology, Govt. of India, and the KLC Memorial Distinguished Lecture Award (2023) by IIT Delhi.

Regards

Avinash

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Regards,

Avinash Lahgere

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