Capacitance Modeling in Dual Field-Plate Power GaN HEMT for Accurate Switching Behavior

Sheikh Aamir Ahsan, *Graduate Student Member, IEEE*, Sudip Ghosh, Khushboo Sharma, Avirup Dasgupta, *Graduate Student Member, IEEE*, Sourabh Khandelwal, *Member, IEEE*, and Yogesh Singh Chauhan, *Senior Member, IEEE*

***Abstract*— In this paper, a surface-potential-based compact model is proposed for the capacitance of an AlGaN/GaN high-electron mobility transistor (HEMT) dual field-plate (FP) structure, i.e., with gate and source FPs. FP incorporation in a HEMT gives an improvement in terms of enhanced breakdown voltage, reduced gate leakage, and so on, but it affects the capacitive nature of the device, particularly by bringing into existence in a subthreshold region of operation, a feedback miller capacitance between the gate and the drain, and also a capacitance between the drain and the source, therefore, affecting switching characteristics. Here, we model the bias dependence of the terminal capacitances, wherein the expressions developed for intrinsic charges required for capacitance derivation are analytical and physics-based in nature and valid for all regions of device operation. The proposed model, implemented in Verilog-A, is in excellent agreement with the measured data for different temperatures.**

***Index Terms*— Capacitance, field plate (FP), GaN high-electron mobility transistors (HEMTs), modeling, surface potential (SP).**

I. Introduction

OVER the last decade, AlGaN/GaN high-electron mobility transistors (HEMTs) have been widely investigated, and they have asserted their dominance in power converters and high-voltage power switches [1]–[3]. It was demonstrated that after incorporating a field-plate (FP) structure in a HEMT, its breakdown voltage (V_{br}) increases, which could be maximized with the proper optimization of FP length and insulator thickness [4]. Although FP-HEMTs exhibit lower unity current gain frequency (f_T) due to increased gate-to-drain (C_{gd}) and drain-to-source (C_{ds}) capacitances due to incorporation of gate-connected FP (GC-FP) and source-connected FP, respectively, they show improved breakdown voltage, linearity, stability, reliability, and efficiency [5].

Manuscript received September 22, 2015; revised November 24, 2015; accepted November 27, 2015. Date of publication December 17, 2015; date of current version January 20, 2016. This work was supported in part by the Indian Space Research Organization, in part by the Ramanujan Fellowship Research Grant, and in part by the DST Fast-Track Scheme for young scientists. The review of this paper was arranged by Editor K. J. Chen.

S. Aamir Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, and Y. S. Chauhan are with the Nanolab, Department of Electrical Engineering, IIT Kanpur, Kanpur 208016, India (e-mail: ahsan@iitk.ac.in; sudip@iitk.ac.in; khushb@iitk.ac.in; avirup@iitk.ac.in; chauhan@iitk.ac.in).

S. Khandelwal is with the Department of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA 94720-2284 USA (e-mail: sourabhkhandelwal@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2015.2504726

So far, an extensive work has been done to enhance V_{br} and to study the effect of optimized FP geometry in further increasing it [6]. Huang *et al.* [7] studied the impact of FPs on trapping behavior and current collapse mitigation, while Chiu *et al.* [8] investigated the impact of varying the length of FPs and gate-to-drain extensions on electrical characteristics. The literature though is lacking in finer details regarding the impact of FPs on the capacitances [9], [10]. Recently, Zhang *et al.* [11] modeled the capacitances for AlGaN/GaN HEMTs, but in their analysis, they did not consider the impact of FPs.

The terminal capacitances, i.e., the input (Ciss), reverse (Crss), and output (Coss) capacitances, determine the power losses in power switching circuits [12]. The C–V profiling gives an idea about the distribution of charge carriers within the material. In addition, in order to maximize the utility of these devices in high-frequency switching circuits, their accurate and speedy simulation is needed. Both these metrics of circuit simulation, i.e., the accuracy and speed, are determined by the compact model describing the device. A lot of models have been proposed for GaN HEMTs, but they are not physics-based in nature [13], [14]. Physics-based models demonstrated earlier made extensive use of numerical techniques for calculation, hence making computation slower [15], while other models were based on MOSFET's equations and ignored the quantum nature of the Two-dimensional electron gas (2-DEG) [16]. This is our primary motivation to go for a physics-based model, which has an intrinsic advantage of having less parameter. The parameters are directly or indirectly linked to the physical effects governing the device dynamics. Hence, their extraction in a physics-based model is relatively easier than in the other models.

In [17]–[19], we analytically modeled the surface-potential (SP) for AlGaN/GaN HEMTs and used this SP to calculate charge and drain current in the device. The model is physics-based, geometrically scalable, showed very good agreement with experimental data, and passed quality benchmarking tests, such as Gummel symmetry, ac symmetry, and harmonic balance, testifying its excellent accuracy and robustness [19]. It is named the Advanced SPICE Model for HEMT (ASM-HEMT) and is one of the two models being evaluated in the final phase of the compact model coalition standardization process and the other one being the MIT Virtual-Source GaN HEMT model [20]. Based on this model, we have so

0018-9383 © 2015 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

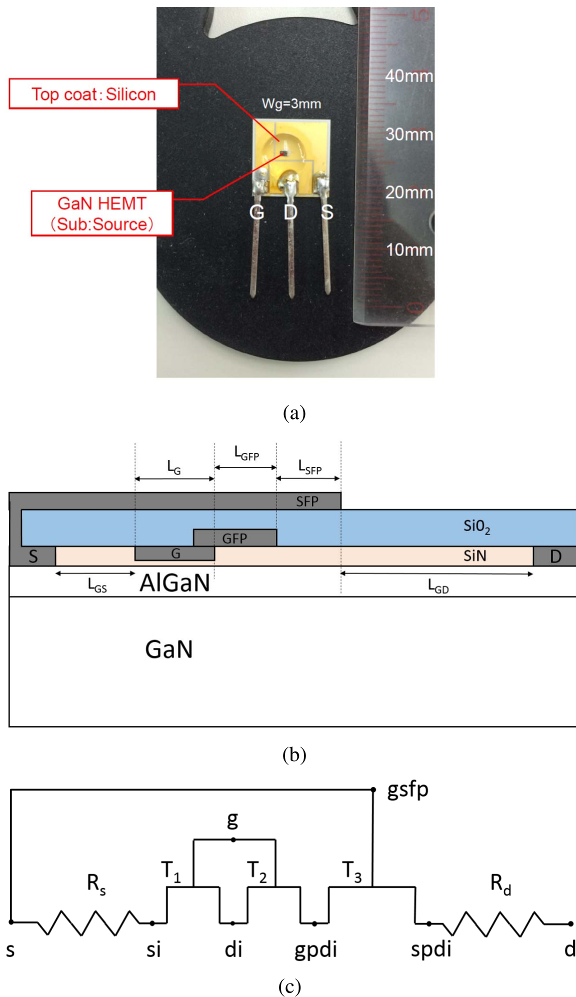


Fig. 1. (a) Dual FP GaN HEMT device which is used as the DUT for capacitance data measurement. (b) Cross-sectional view of the dual FP device showing the gate and source FPs and their appropriate connections to gate and source, respectively. The device dimensions are $L_G = 1$ μm, $W = 3$ mm, $L_{\text{GFP}} = L_{\text{SFP}} = 3.5$ μm, $L_{\text{GS}} = 2$ μm, and $L_{\text{GD}} = 12$ μm. (c) Model representation of the device. T_1, T_2, and T_3 denote intrinsic, gate FP, and source FP transistors, respectively. The intrinsic nodes within the device are also indicated.

far modeled flicker noise, thermal noise, and gate current in AlGaN/GaN HEMTs [21]–[23], in addition to the core modeling of dc-IV, intrinsic capacitances, and so on, and now aim to present the capacitance model for a dual FP power GaN HEMT. To the best of our knowledge, this is the first time an SP-based model for FP capacitance in AlGaN/GaN HEMTs is reported.

This paper is organized as follows. Section II describes the modeling of capacitances for an FP HEMT. The results of our proposed model are discussed in Section III. A circuit simulation using the developed model is discussed in Section IV to show the impact of FPs on circuit behavior. Finally, the conclusion is drawn in Section V.

II. Model Description

A. Dual Field-Plate Device Abstraction

Fig. 1(a) shows the gate and source FP AlGaN/GaN HEMT put on direct copper bond board. Fig. 1(b) shows a not-to-the-scale cross-sectional view of the same device. It has a layered MIS-HEMT structure with a thin epitaxial AlGaN film placed on GaN, forming the AlGaN/GaN heterojunction between them. Metallic electrodes are used for gate, source, and drain contacts as well as for the GC-FP and SC-FP.

The 2-DEG charge, which is formed at the heterojunction due to the combined effect of conduction band discontinuity and spontaneous and piezoelectric polarization in the AlGaN/GaN system, gets modulated in the region directly under the GC-FP due to the vertical field originating from it. The cutoff voltage (V_{OFF}) needed at the GC-FP to deplete the 2-DEG at the heterojunction corresponds to the equivalent thickness of the AlGaN barrier layer and insulator upon which the GC-FP rests. Up to a certain limit, thicker the equivalent barrier with the dielectric same as AlGaN, more negative will be the V_{OFF} for the GC-FP [6]. The same is true for the SC-FP. Transistor properties to GC-FP and SC-FP can, therefore, be assigned due to their 2-DEG controlling ability. This forms the basis of our model as shown in Fig. 1(c), where the whole device is represented as a series combination of three independent HEMTs—the intrinsic transistor (T_1), the gate FP transistor (T_2), and the source FP transistor (T_3) and two resistors—the gate–source and gate–drain access region resistances R_s and R_d, respectively. We obtain the SP for each of these transistors separately as explained in Section II-B, from which we evaluate intrinsic charges for each transistor required to find the capacitances. The model displays temperature scaling of its parameters that have a role to play in the temperature dependence of the model, in a way such that there is only a single global parameter set governing the model. For the sake of generality and in order to avoid redundancy in description, the model variables and the parameters have been represented with a subscript k, where k is 1 for equations corresponding to T_1, 2 for T_2, and 3 for T_3. We represent the direction along the channel from source to drain by the x-axis.

B. Surface Potential and Intrinsic Charge Calculation

The calculation of the small signal capacitance of a device demands the precise evaluation of the charges that get developed at the various nodes of the device on application of some small signal voltage. These charges are calculated in terms of SP (ψ), which we comprehensively demonstrated in [17]–[19].

We self-consistently solve the triangular quantum well formed at the heterojunction for its eigenvalues using Schrodinger's and Poisson's equations. Considering the two important subbands E_0 and E_1 to be occupied, we use Fermi–Dirac statistics to obtain the 2-DEG charge density for each of the three transistors T_1, T_2, and T_3. Solutions for the quasi-Fermi level (E_F) are obtained for each of the regions of V_g sweep in terms of V_{go} ($Vg - V_{\text{OFF}}$), and a unified expression for E_F is reproduced from [18] for the sake of convenience as under

$$E_{F,k} = V_{\text{go},k} - \frac{2V_{\text{th}} \ln\left(1 + e^{\frac{V_{\text{go},k}}{2V_{\text{th}}}}\right)}{1/H(V\text{go}, p) + (C_{g,k}/qD)e^{-\frac{V_{\text{go},k}}{2V_{\text{th}}}}}. \quad (1)$$

An iterative reevaluation of E_F using Householder's method [24] is done for better accuracy. E_F allows us to

calculate the SP ($\psi_k = E_{F,k} + V_{x,k}$) at both ends of the channel as $\psi_{s,k} = E_{F,k}$ and $\psi_{d,k} = E_{F,k} + V_{\mathrm{ds},k}$, where $V_{\mathrm{ds},k}$ is the drain–source voltage for transistor T_k. The overall device SP, which is spatially divided into the SP for each of the modeled transistors, is stitched in a continuous fashion by the SPICE simulator.

In order to obtain the capacitances of the device, the intrinsic charges at source (Q_s), drain (Q_d), and gate (Q_g) for each of the modeled transistors are to be accurately evaluated. The following equation gives the gate charge:

$$Q_{g,k} = -\int_0^{L_k} WC_{g,k}(V_{\mathrm{go},k} - \psi_k(x))dx \tag{4}$$

where $C_{g,k} = (\epsilon_k/d_k)$ is the gate capacitance per unit area. d_k is the insulator thickness, while W and L_k are the channel width and channel length of the transistor T_k, respectively. Integrating (4), we get the total gate charge given by (2), as shown at the bottom of this page. T is the device operating temperature and K_B is the Boltzmann constant.

$Q_{d,k}$ and $Q_{s,k}$ are found using the position and gate-bias-dependent channel charge per unit length given by $Q_{\mathrm{ch},k}(V_{\mathrm{go},k}, V_{x,k}) = WC_{g,k}(V_{\mathrm{go},k} - \psi(x))$. This charge is partitioned by the Ward–Dutton scheme, wherein the drain and source charges are defined as $Q_{d,k} = \int_0^{L_k}(x/L_k)Q_{\mathrm{ch},k}dx$ and $Q_{s,k} = \int_0^{L_k}(1 - x/L_k)Q_{\mathrm{ch},k}dx$, respectively [25]. Using the expression for $Q_{\mathrm{ch},k}$, a drain charge can be calculated by the integral

$$Q_{d,k} = \int_0^{L_k}(x/L_k)WC_{g,k}(V_{\mathrm{go},k} - \psi_k(x))dx \tag{5}$$

which upon further transformation results into (3), as shown at the bottom of this page.

Charge conservation maintained between the gate, drain, and source terminals allows us to obtain the source charge using (2) and (3) as

$$Q_{s,k} = -Q_{g,k} - Q_{d,k}. \tag{6}$$

C. Capacitance Calculation

In order to comprehend the dynamic behavior of the FP HEMT device, there is a need to examine the charging and discharging of the various internal capacitances within the device. Therefore, our task understandably would be to model the gate-to-source (C_{gs}), gate-to-drain (C_{gd}), and drain-to-source (C_{ds}) capacitances between the terminal nodes of the HEMT device with FPs. However, the data that are commonly provided are the bias dependence of terminal capacitances Ciss, Crss and Coss, which are defined as

$$\mathrm{Crss} = C_{\mathrm{gd}} \tag{7}$$

$$\mathrm{Ciss} = C_{\mathrm{gd}} + C_{\mathrm{gs}} \tag{8}$$

$$\mathrm{Coss} = C_{\mathrm{gd}} + C_{\mathrm{ds}}. \tag{9}$$

TABLE I

CHARGES AT INTRINSIC NODES OF THE THREE TRANSISTORS

Terminal \ Transistor	T_1	T_2	T_3
Gate	$q_{g1}(g)$	$q_{g2}(g)$	$q_{g3}(s)$
Source	$q_{s1}(si)$	$q_{s2}(di)$	$q_{s3}(gpdi)$
Drain	$q_{d1}(di)$	$q_{d2}(gpdi)$	$q_{d3}(spdi)$

Having obtained the intrinsic charges for the three transistors, we assign them in accordance with Fig. 1(c) to the intrinsic nodes within the device (in parenthesis), as shown in Table I. It must be noted that the gate charge for T_3 is assigned to the source node s due to the connection between nodes gsfp and s. We are now in a position to compute all the nonreciprocal device capacitances from the definition

$$C_{mn} = \pm(dQ_m/dV_n) \tag{10}$$

where $\pm$ is $+$ for $m = n$ and $-$ for $m \neq n$.

It is important to consider the capacitances due to the access regions, particularly at the drain end C_{accd} due to the extension of the depletion region on the drain end. C_{accd} shows up in C_{ds}, in the form of a depletion capacitance, tailing off gradually for higher drain voltages. We formulate it as

$$C_{\mathrm{accd}} = \frac{C_{J0}}{\left(1 + \frac{V_{\mathrm{ds}}}{V_{\mathrm{bi}}}\right)^{\mathrm{MZ}}} \tag{11}$$

where V_{bi} is taken as a parameter. MZ controls the way with which the junction capacitance decays with drain bias and C_{J0} is a parameter that governs the low bias depletion capacitance. Since, at low values of V_{ds}, C_{ds} primarily is a bias-independent capacitance due to the incorporation of the SC-FP, a parameter AJ is used in restricting C_{accd} at low drain voltages, using the MIN function.

There exists a parallel plate capacitance between the gate/GC-FP and the overlying SC-FP. This bias-independent capacitance is taken care of by introducing a parameter CFG into the model, which adjusts the minimum value of C_{gs}.

$$Q_{g,k} = -WL_kC_{g,k}\left\{V_{\mathrm{go},k} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k}) + \frac{(\psi_{d,k} - \psi_{s,k})^2}{12\left(V_{\mathrm{go},k} - \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k})\right)^2}\right\} \tag{2}$$

$$Q_{d,k} = -\frac{1}{2}WL_kC_{g,k}\left\{V_{\mathrm{go},k} - \frac{1}{3}(\psi_{s,k} + 2\psi_{d,k}) + \frac{1}{12}\left(\frac{\psi^2_{\mathrm{ds},k}}{\left(V_{\mathrm{go},k} + \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k})\right)}\right) + \frac{1}{12}\psi^3_{\mathrm{ds},k}\left(V_{\mathrm{go},k} + \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k})\right)^2\right\} \tag{3}$$

D. Temperature Dependence

Our model accounts for the temperature scaling of its parameters that have a role to play in the temperature dependence of the model, leading us to a single parameter set for temperature ranges 25 °C–150 °C. Temperature dependence in our capacitance model for a GaN HEMT with FPs primarily comes about due to variation in $V_{\mathrm{OFF},k}$ with T. According to [26]

$$V_{\mathrm{OFF}}(T) = \phi_B - \Delta E_c(T) - \frac{\sigma_{\mathrm{pz}}(T)d}{\epsilon} - \frac{qN_d d^2}{2\epsilon} \tag{12}$$

where ΔE_c is the discontinuity in conduction band between AlGaN/GaN, ϕ_B represents the Schottky barrier, σ_{pz} gives the interface charge density induced due to polarization, and d, ϵ, and N_d are the AlGaN layer material parameters carrying usual meaning. The doping density N_d is negligible, since AlGaN is undoped in our case. $\sigma_{\mathrm{pz}}(T)$ is a very weak function of temperature and its temperature variation can be ignored to the first-order approximation. ΔE_c, being a function of the energy bandgaps of AlGaN ($E_g^{\mathrm{AlGaN}}(T)$) and GaN ($E_g^{\mathrm{GaN}}(T)$), varies strongly with T as given by [27]

$$\Delta E_c = 0.70\big(E_g^{\mathrm{AlGaN}}(T) - E_g^{\mathrm{GaN}}(T)\big). \tag{13}$$

With these simplifications, we model V_{OFF} as a linearly varying function of temperature as demanded by the trend shown in experimental data. It is given as [28]

$$V_{\mathrm{OFF},k}(T) = V_{\mathrm{OFF},k} - V_{\mathrm{temp},k}\left(\frac{T}{T_{\mathrm{NOM}}} - 1\right) \tag{14}$$

where $V_{\mathrm{temp},k}$ is the V_{OFF} temperature dependence parameter for transistor T_k. The parenthesized T denotes the temperature scaling of the parameter at device operating temperature T, while T_{NOM} is the nominal temperature set to 25 °C.

C_{ds} shows a variable decay at high drain bias with temperature as is observed from the experimental data. In order to model that we employ temperature dependence for built in voltage V_{bi} and the-bias independent depletion capacitance parameter C_{J0} given as

$$V_{\mathrm{bi}}(T) = V_{\mathrm{bi}} - V_{\mathrm{temp,VBI}}\left(\frac{T}{T_{\mathrm{NOM}}} - 1\right) \tag{15}$$

$$C_{J0}(T) = C_{J0} - V_{\mathrm{temp},CJ0}\left(\frac{T}{T_{\mathrm{NOM}}} - 1\right) \tag{16}$$

where $V_{\mathrm{temp,VBI}}$ and $V_{\mathrm{temp},CJ0}$ are parameters for V_{bi} and C_{J0} temperature scaling.

III. Parameter Extraction, Results, and Discussion

Table II shows the description of the model parameters along with their extracted values. We begin the $V_{\mathrm{OFF},k}$ parameter extraction process for device by fitting our model results for V_{gs} dependence of Ciss with the experimental data at $V_{\mathrm{ds}} = 0$ V, as shown in Fig. 2(a). The figure also shows C_{gd} and C_{gs}, which are the individual capacitance components that sum up and give Ciss. Two humplike features are seen to arise at transition regions that represent V_{OFF1} and V_{OFF2} as pointed out in the plot. Gate length $L_{1,2}$ and insulator thickness $d_{1,2}$ for $T_{1,2}$ determine the magnitude of the two humplike features in Fig. 2(a). Greater the gate length, greater would be the capacitance, and vice versa for insulator thickness. Here, geometrical device parameters have been used. The parallel plate capacitance parameter CFG controls the bias-independent value of Ciss for sufficiently negative V_{gs}. It must be noted that due to the absence of an electrical connection between the nodes gsfp and g, no contribution from T_3 is made either to C_{gs} or C_{gd}, even though T_3 remains ON for all V_{gs} values in Fig. 2(a). Therefore, for parameters corresponding to T_3, we rely on the other modeling results.

TABLE II
Parameters for Dual FP HEMT Capacitance Model

Parameter	Description	Extracted Value/Remarks
k	Subscript used as index for different transistors	1 for T_1, 2 for T_2 and 3 for T_3
$TNOM$	Nominal temperature (° C)	25
$V_{off,k}$	Cutoff Voltage (V)	V_{off1}=−3, V_{off2}=−51, V_{off3}=−75
L_k	Gate length (μm)	L_1=1, L_2=3.5, L_3=3.5
d_k	Insulator thickness (μm)	d_1=0.04, d_2=0.35, d_3=2
CFG	Parallel Plate Capacitance parameter (pF)	5.8
$V_{temp,k}$	For $V_{off,k}$ temperature depencence (V)	$V_{temp,1}$=9.86, $V_{temp,2}$=6.19, $V_{temp,3}$=49.39
V_{bi}	Built in voltage (V)	0.877
$V_{temp,VBI}$	For V_{bi} temperature depencence (V)	0.297
MZ	Determines the decay in C_{ds} with V_{ds}	0.744
C_{J0}	Decides the zero V_{ds} depletion capacitance (pF)	64.15
$V_{temp,CJ0}$	For $CJ0$ temperature depencence (pF)	6.884
AJ	For restricting C_{ds} at low V_{ds} (pF)	3.67

Fig. 2(b) shows the formation of 2-DEG in transistors T_1, T_2, and T_3 as a function of V_{gs}. V_{ds} is fixed at 0 V, forcing the voltages at intrinsic nodes si, di, gpdi, and spdi to 0 V. Since the AlGaN/GaN HEMT is a normally ON device due to its conduction band profile and polarization induction, it needs negative gate voltage in order to turn it OFF. The insulator thickness for T_2 is greater than for T_1, and therefore, it requires a more negative voltage at its gate in order to deplete the 2-DEG. It is seen that the cutoff voltages for $T_1(V_{\mathrm{OFF1}})$ and $T_2(V_{\mathrm{OFF2}})$, according to our model, fall around −3 and −51 V, respectively, as these are the voltage values where 2-DEG starts to build up within the transistor. The same values for cutoff voltages are seen in Fig. 2(a). T_3 has a greater insulator thickness than T_2, as shown in Fig. 1(b), so a logical extrapolation of the above analysis would suggest an even more negative cutoff voltage (V_{OFF3}) for T_3. It must be noted that the gate (gsfp) of T_3 is connected to the source node (s) of the overall HEMT device due to the connection between the source and the source FP, as shown in Fig. 1(b). Therefore, the gate–source voltage (V_{gs3}) for T_3 is clamped to 0 V. This keeps T_3 in the ON-state with

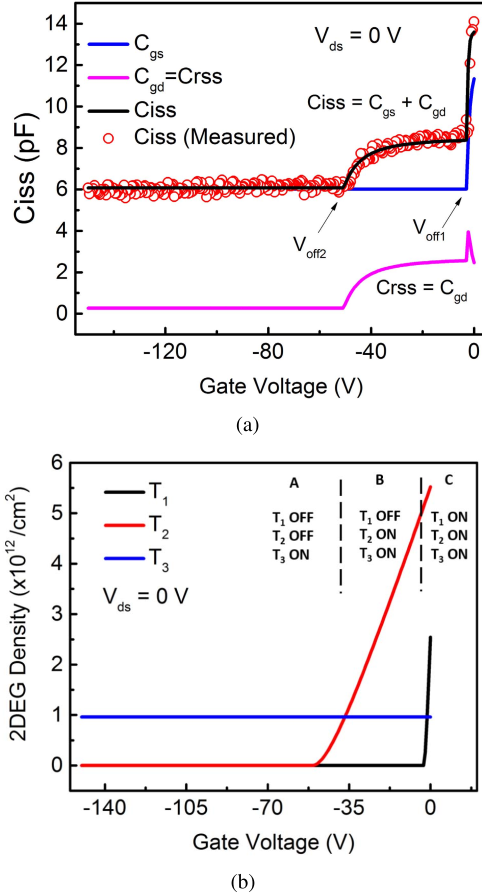


Fig. 2. (a) Comparison of the modeled Ciss $-$ V_{gs} with experimental data. V_{ds} is fixed at 0 V. C_{gs} and C_{gd}, that together add up to give Ciss, have also been plotted. (b) 2-DEG density for transistors T_1, T_2, and T_3 as a function of V_{gs}, illustrating cutoff voltages for transistors T_1 and T_2 to be -51 and -3 V, respectively. It is seen that T_3 is ON throughout the V_{gs} sweep. Regions A, B, and C for V_{gs} operation have also been indicated.

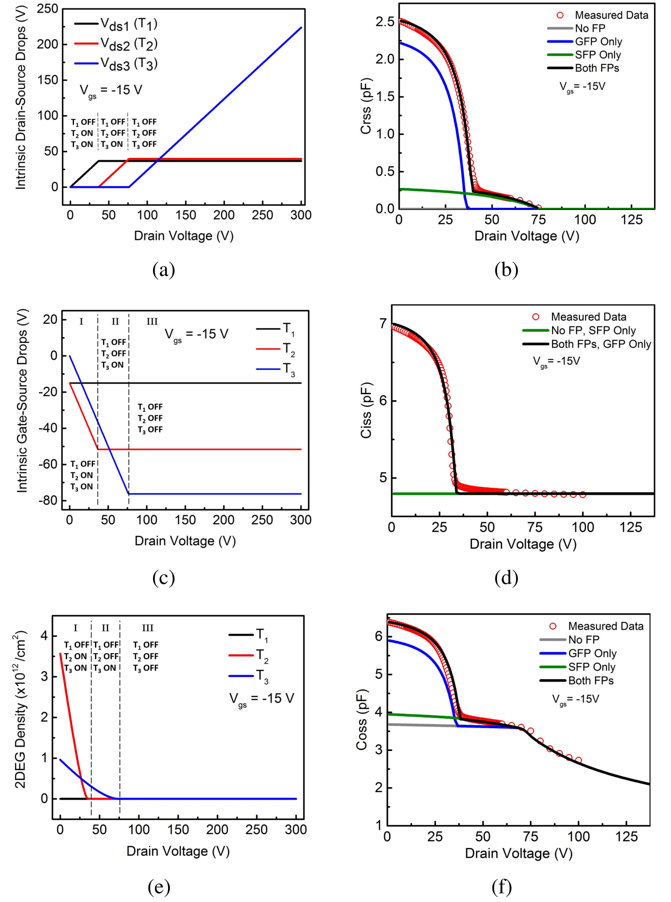


Fig. 3. Variation of (a) intrinsic drain–source voltages, (c) intrinsic gate–source voltages, and (e) 2-DEG density for transistors T_1, T_2, and T_3 with V_{ds} under subthreshold conditions, i.e., $V_{\mathrm{gs}} = -15$ V. Regions I, II, and III for V_{ds} operation have also been indicated. Comparison of the modeled (b) Crss, (d) Ciss, and (f) Coss capacitances with experimental data. Contributions made by both the FPs in conjunction with the intrinsic device are also shown. Solid lines are used for model simulations.

a substantial 2-DEG as shown in Fig. 2(b), independent of the overall V_{gs} values. The entire V_{gs} sweep in Fig. 2(b) is divided into three regions, namely, regions A, B, and C based on the ON/OFF condition of intrinsic transistors.

In Fig. 3(a) and (c), we show the V_{ds} dependence of the intrinsic drain–source voltage $V_{\mathrm{ds},k}$ and intrinsic gate–source voltages $V_{\mathrm{gs},k}$, respectively, for transistors T_k, where k represents the transistor index. In Fig. 3(e), we plot the 2-DEG variation for transistor T_k with V_{ds}. All the plots in Fig. 3 are coherent and together indicate the ON/OFF condition of transistors for different regions of V_{ds}.

All the parameters corresponding to T_3, whose extraction could not be made from results in Fig. 2(a), can now be extracted by V_{ds} dependence of Ciss, Crss, and Coss under a subthreshold condition, as shown in Fig. 3(b), (d), and (f). The contributions of GC-FP and SC-FP in conjunction with the intrinsic device toward terminal capacitances are shown. V_{OFF3} is extracted from the overall V_{ds} dropped almost entirely across T_1 and T_2, at which SC-FP begins to contribute toward Crss, as shown in Fig. 3(b). Its value comes out to be $V_s - V_{\mathrm{gpdi}} = -75$ V.

In Fig. 4, modeled capacitance results are shown for FP devices with two different widths, i.e., $W = 3$ mm and $W = 6$ mm, thereby highlighting the scalable property of the model, which can be ascribed to its physical nature. The individual components to the terminal capacitances, i.e., C_{gs}, C_{ds}, and C_{gd}, have also been plotted.

Finally, we have validated our model for the temperature dependence of the above-mentioned terminal capacitances in Fig. 5. Increase in temperature causes V_{OFF1} to decrease as shown in Fig. 5(a), and has been modeled in (14). The primary reason for V_{OFF1} variation is decrease in ΔE_c with increase in temperature as explained in (12) and (13). In Fig. 5(b)–(d), temperature dependence is reflected in a decrease of $V_{\mathrm{OFF2,3}}$ for higher temperatures, causing the capacitance humps to shift leftward. $V_{\mathrm{temp,1,2}}$ is extracted from these plots. The depletion capacitance temperature parameters $V_{\mathrm{temp,VBI}}$ and $V_{\mathrm{temp},CJ0}$ are extracted from Fig. 5(d).

IV. Circuit Simulation Using Model

We performed a transient simulation in an Advanced Design System (ADS) circuit simulator to get a flavor of the switching characteristics. Our above developed model in the form of a Verilog-A code was installed in the ADS design kit for simulating the behavior of the

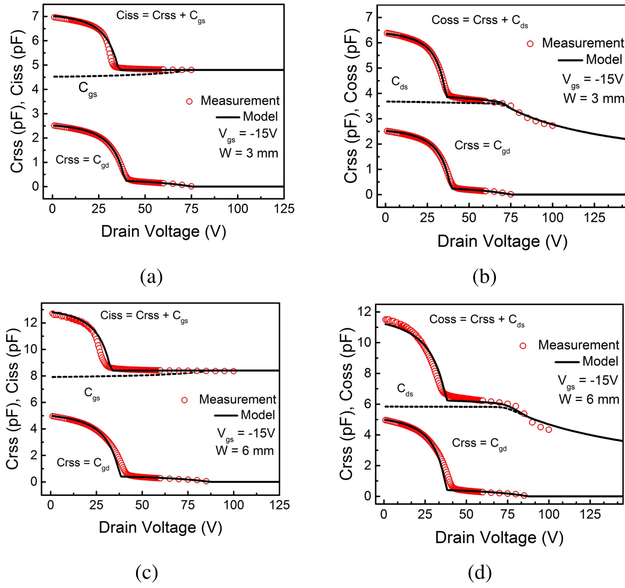


Fig. 4. Comparison of the modeled (a) Ciss$-V_{\rm ds}$ and (b) Coss$-V_{\rm ds}$ with experimental data under subthreshold conditions for device with $W = 3$ mm. $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ have also been plotted in order to show their contributions to the terminal capacitances under various regions of $V_{\rm ds}$ operation. Corresponding plots for device with $W = 6$ mm are shown in (c) and (d), respectively.

device. The FP capacitance model parameters, as shown in Table II, were loaded in the design kit in addition to the ASM-HEMT core model parameters. The demo circuit schematic shown in Fig. 6(a) is chosen, such that the switching behavior of the device during pulsed excitation at the gate is reflected at the switch node, i.e., the output node. The dual FP HEMT device is the device under test (DUT) along with a load resistor (R) and inductor (L), and their values have been chosen in a manner to obtain observable transients (rise and fall times) in comparison with the pulsewidth. The excitation at the gate is provided by a 2.5-MHz pulse waveform going from −15 V (subthreshold) to 0 V (ON-state), with a pulsewidth of 200 ns and 50% duty cycle. The drain bias of 10 V and 300 V is applied separately to observe the behavior at high and low biases. The results of the transient simulation are shown in Fig. 6(b).

As is seen, during turn ON, the slew rate ($\mathrm{SR_{ON}} = (dV_{\rm OUT}/dt)$) at the output node depends inversely upon $C_{\rm gd}$, i.e., $\mathrm{SR_{ON}} \propto (I_g/C_{\rm gd})$. Since $C_{\rm gd}$ at low $V_{\rm ds}$ for the FP device is much more than for the device without the FP, we see a degradation in $\mathrm{SR_{ON}}$ due to FP implementation for $V_{\rm DD} = 10$ V. For high $V_{\rm ds}$, since $C_{\rm gd}$ is the same for both the cases (with and without FP), we do not see any notable change in the turn-ON transient at $V_{\rm DD} = 300$ V. During the turn-OFF transient, the device is pushed into a subthreshold region and ringing is observed at the falling edge before it finally damps down. It is due to the charging of the Coss capacitance at the drain node of the device, which in combination with L and R forms the series RLC circuit. The turn-OFF slew rate ($\mathrm{SR_{OFF}}$) is an inverse function of Coss, given as ($\mathrm{SR_{OFF}} \propto (I_d/\mathrm{Coss})$), since the output current charges the Coss capacitor during turn-OFF. The reduction in $\mathrm{SR_{OFF}}$ is severe for lower drain bias values, while it remains unchanged at high drain bias due to the same Coss value for with and without FP cases which goes in accordance with Fig. 4(b).

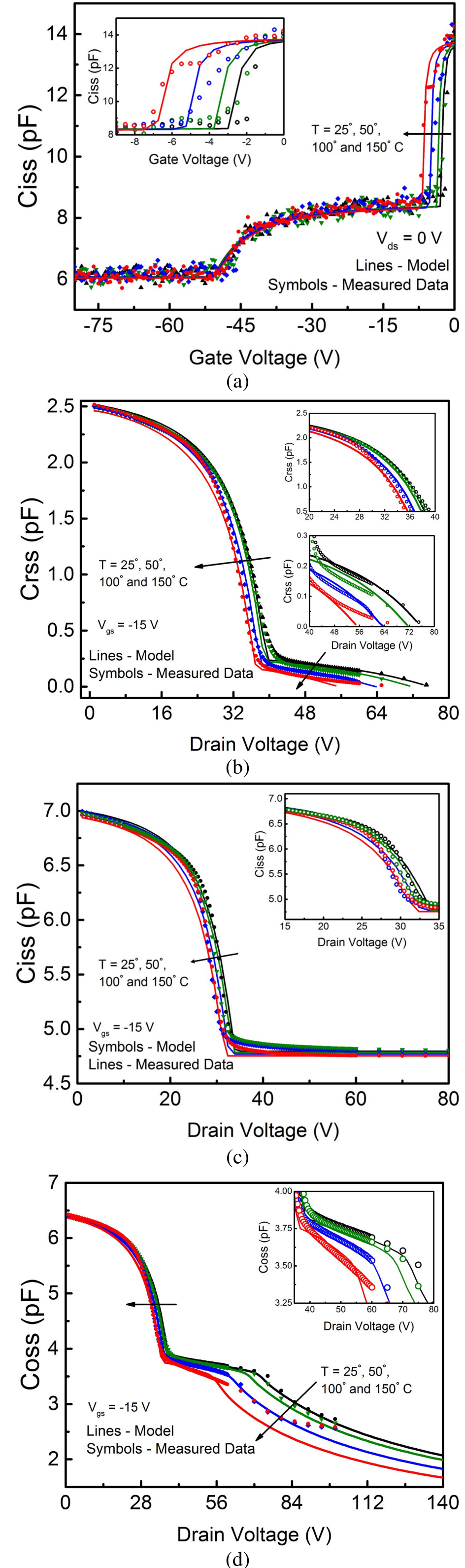
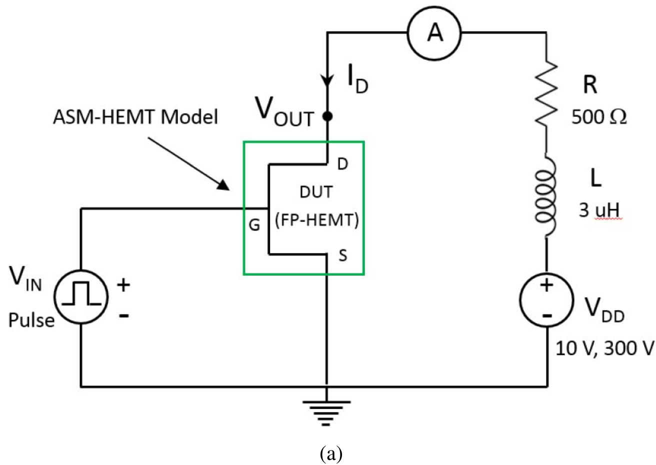
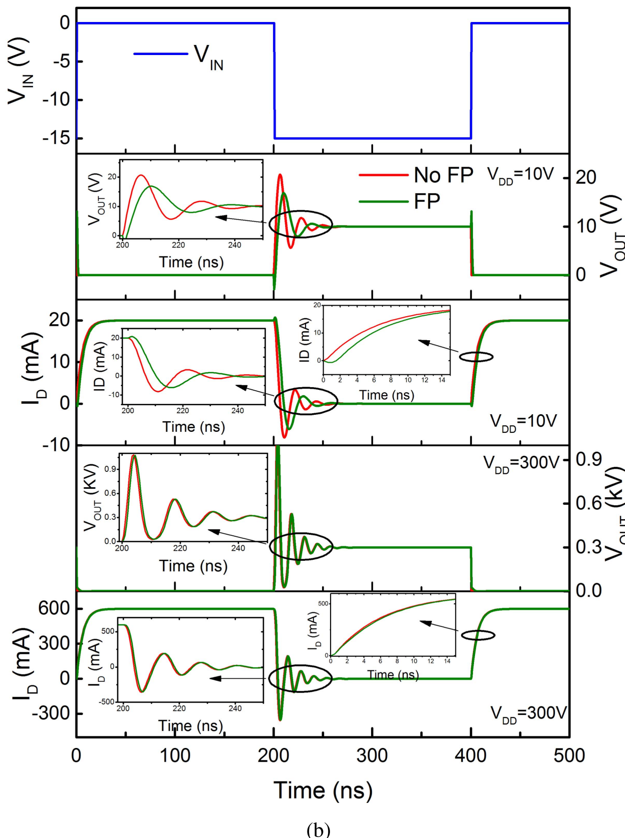


Fig. 5. Temperature dependence of (a) Ciss$-V_{\rm gs}$, (b) Crss$-V_{\rm ds}$, (c) Ciss$-V_{\rm ds}$, and (d) Coss$-V_{\rm ds}$ is shown for 25°, 50°, 100°, and 150°. Insets: temperature sensitive ranges have been added for better clarity. Extracted values of temperature dependence parameters $V_{\mathrm{temp},k}$, $V_{\mathrm{temp,VBI}}$, and $V_{\mathrm{temp},CJ0}$ are given in Table II.



(a)



(b)

Fig. 6. (a) Schematic for ADS circuit simulation using developed model. The FP-HEMT is put as the DUT with −15 and 0 V pulses of 200-ns pulsewidth and 50% duty cycle at gate and a resistive load at the drain. ASM-HEMT model Verilog code is used for simulating the circuit behavior using ADS design kit with model parameters presented in Table II. (b) Transient simulation results. Input pulse (V_{IN}), output voltage (V_{OUT}), and current I_D have been shown. Results are shown for $V_{\mathrm{DD}} = 10$ V and 300 V. Insets: zoomed-in view for better clarity. Degradations in $\mathrm{SR}_{\mathrm{ON}}$ and $\mathrm{SR}_{\mathrm{OFF}}$ due to FP incorporation are observed for low drain biases because of increased C_{gd} and Coss values, respectively.

V. Conclusion

To summarize, an SP-based model for the capacitances in a HEMT device with gate and source FPs has been developed. The model is physics-based and essentially predicts the contributions due to FP incorporation and captures well the transition regions in the C–V behavior. The feedback transcapacitance C_{gd} and the drain–source capacitance C_{ds} under subthreshold conditions due to GC-FP and SC-FP, respectively, are observed, which show their presence in the terminal capacitances of the device. The model is validated against the experimental data for two different gate widths, and excellent fits are obtained. Finally, an ADS transient simulation is performed with a demo circuit in order to highlight the significance of modeling the terminal capacitances required for a transient simulation based on dual FP power GaN HEMTs.

Acknowledgment

The authors would like to thank Toshiba for providing the experimental data as a part of Si2-CMC model standardization activity.

References

[1] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, “An assessment of wide bandgap semiconductors for power devices,” *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, May 2003.

[2] U. K. Mishra, P. Parikh, and Y.-F. Wu, “AlGaN/GaN HEMTs—An overview of device operation and applications,” *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[3] X. Huang, Z. Liu, Q. Li, and F. C. Lee, “Evaluation and application of 600 V GaN HEMT in cascode structure,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[4] Y.-F. Wu *et al.*, “30-W/mm GaN HEMTs by field plate optimization,” *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004.

[5] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, “GaN-based RF power devices and amplifiers,” *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[6] S. Karmalkar and U. K. Mishra, “Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate,” *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, Aug. 2001.

[7] H. Huang, Y. C. Liang, G. S. Samudra, T.-F. Chang, and C.-F. Huang, “Effects of gate field plates on the surface state related current collapse in AlGaN/GaN HEMTs,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2164–2173, May 2014.

[8] H.-C. Chiu, C.-W. Yang, H.-C. Wang, F.-H. Huang, H.-L. Kao, and F.-T. Chien, “Characteristics of AlGaN/GaN HEMTs with various field-plate and gate-to-drain extensions,” *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3877–3882, Nov. 2013.

[9] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, “High breakdown voltage AlGaN–GaN HEMTs achieved by multiple field plates,” *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 161–163, Apr. 2004.

[10] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, “High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates,” *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 713–715, Sep. 2006.

[11] A. Zhang *et al.*, “Analytical modeling of capacitances for GaN HEMTs, including parasitic components,” *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 755–761, Mar. 2014.

[12] X. Huang, Q. Li, Z. Liu, and F. C. Lee, “Analytical loss model of high voltage GaN HEMT in cascode configuration,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.

[13] I. Angelov *et al.*, “Large-signal modelling and comparison of AlGaN/GaN HEMTs and SiC MESFETs,” in *Proc. Asia-Pacific Microw. Conf.*, Dec. 2006, pp. 279–282.

[14] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, “Modeling GaN: Powerful but challenging,” *IEEE Microw. Mag.*, vol. 11, no. 6, pp. 82–96, Oct. 2010.

[15] A. Koudymov *et al.*, “Analytical HFET I–V model in presence of current collapse,” *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 712–720, Mar. 2008.

[16] D. L. John, F. Allerstam, T. Rödle, S. K. Murad, and G. D. J. Smit, “A surface-potential based model for GaN HEMTs in RF power amplifier applications,” in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2010, pp. 8.3.1–8.3.4.

[17] S. Khandelwal, Y. S. Chauhan, and T. A. Fjeldly, “Analytical modeling of surface-potential and intrinsic charges in AlGaN/GaN HEMT devices,” *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2856–2860, Oct. 2012.

[18] S. Khandelwal and T. A. Fjeldly, "A physics based compact model of I–V and C-V characteristics in AlGaN/GaN HEMT devices," *Solid-State Electron.*, vol. 76, pp. 60–66, Oct. 2012.

[19] S. Khandelwal *et al.*, "Robust surface-potential-based compact model for GaN HEMT IC design," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3216–3222, Oct. 2013.

[20] U. Radhakrishna *et al.*, "High voltage GaN HEMT compact model: Experimental verification, field plate optimization and charge trapping," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2013, pp. 32.7.1–32.7.4.

[21] A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Compact Modeling of flicker noise in HEMTs," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 174–178, Aug. 2014.

[22] A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Surface potential based modeling of thermal noise for HEMT circuit simulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 6, pp. 376–378, Jun. 2015.

[23] S. Ghosh, A. Dasgupta, S. Khandelwal, S. Agnihotri, and Y. S. Chauhan, "Surface-potential-based compact modeling of gate current in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 443–448, Feb. 2015.

[24] A. S. Householder, *The Numerical Treatment of a Single Nonlinear Equation*. New York, NY, USA: McGraw-Hill, 1970.

[25] D. E. Ward, "Charge-based modeling of capacitance in MOS transistors," Integr. Circuits Lab., Stanford Univ., Stanford, CA, USA, Tech. Rep. G201-11, Jun. 1981.

[26] M. A. Huque, S. A. Eliza, T. Rahman, H. F. Huq, and S. K. Islam, "Temperature dependent analytical model for current–voltage characteristics of AlGaN/GaN power HEMT," *Solid-State Electron.*, vol. 53, no. 3, pp. 341–348, Mar. 2009.

[27] G. Martin *et al.*, "Valence-band discontinuity between GaN and AlN measured by X-ray photoemission spectroscopy," *Appl. Phys. Lett.*, vol. 65, no. 5, pp. 610–612, Aug. 1994.

[28] Y. S. Chauhan *et al.*, "BSIM6: Analog and RF compact model for bulk MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 234–244, Feb. 2014.

Sheikh Aamir Ahsan (GSM'15) was born in Srinagar, India, in 1988. He received the B.Tech. degree in electronics and communication engineering from the National Institute of Technology Jaipur, Jaipur, India, in 2011. He is currently pursuing the Ph.D. degree with the Nanolab, IIT Kanpur, Kanpur, India.

His current research interests include characterization, compact modeling, and RF circuit design of gallium nitride HEMTs.

Sudip Ghosh received the Ph.D. degree from the University of Bordeaux 1, Bordeaux, France, in 2012, and the M.Sc. degree from Jadavpur University, Kolkata, India, in 2008.

He was a Guest Researcher with the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2013. He is currently a Post-Doctoral Researcher with IIT Kanpur, Kanpur, India.

Khushboo Sharma received the master's degree from the Narsee Monjee Institute of Management Studies, Mumbai, India, in 2015.

She was a Student Research Associate with IIT Kanpur, Kanpur, India, from 2014 to 2015, where she was involved in compact modeling toward the accomplishment of the master's degree.

Avirup Dasgupta (GSM'14) received the B.Tech. and M.Tech. degrees from IIT Kanpur, Kanpur, India, where he is currently pursuing the Ph.D. degree.

His current research interests include compact modeling of semiconductor devices and noise characteristics.

Mr. Dasgupta has authored a quite a few journal and conference papers and was a recipient of multiple awards and scholarships, including the prestigious National Talent Award in 2009.

Sourabh Khandelwal (M'14) received the Ph.D. degree from the Norwegian University of Science and Technology, Trondheim, Norway, in 2013, and the M.Tech. degree from IIT Bombay, Mumbai, India, in 2007.

He was a Research Engineer with IBM Semiconductor Research, Bangalore, India, from 2007 to 2010. He is currently a Post-Doctoral Fellow with the University of California at Berkeley, Berkeley, CA, USA.

Yogesh Singh Chauhan (SM'12) received the Ph.D. degree from the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2007.

He was with IBM, Bangalore, India, from 2007 to 2010, and the University of California at Berkeley, Berkeley, CA, USA, from 2010 to 2012. Since 2012, he has been a Faculty Member with IIT Kanpur, Kanpur, India. His current research interests include characterization, compact modeling, and simulation of advanced semiconductor devices.