GaN HEMT Modeling for Power and RF Applications using ASM-HEMT

Sudip Ghosh*, Sheikh Aamir Ahsan*, Avirup Dasgupta*, Sourabh Khandelwal†, and Yogesh Singh Chauhan*
* Indian Institute of Technology Kanpur, India
† University of California Berkeley, USA
Email: sudip@iitk.ac.in

***Abstract*—In this paper, we aim to present an overview of a surface-potential (SP) based model named "Advanced Spice Model for High Electron Mobility Transistor" (ASM-HEMT) for AlGaN/GaN HEMTs. This model is presently under consideration in the phase-III of industry standardization by the Compact Model Coalition (CMC). SP of GaN HEMT is obtained by solving Schrodinger and Poisson equations in the triangular potential well considering the first two energy subbands. The core drain current model and a intrinsic charge model are derived using the developed SP model. Various real device effects like: velocity saturation, drain-induced barrier lowering (DIBL), self-heating, field dependent mobility, non-linear access region resistances etc. are included in the core drain current model to represent real GaN HEMTs. Field-plate (FP) model is incorporated to predict accurate current and capacitance trends observed in the high power GaN HEMTs with source and gate connected field-plates. Along with the gate current model, non-linear trapping effects are also included in the model to capture large-signal high-frequency device behavior. This model is extensively validated with the experimental data of both high power and high frequency GaN HEMTs.**

***Index Terms*—AlGaN/GaN HEMTs, compact model, ASM-HEMT.**

I. Introduction

Gallium Nitride (GaN) based HEMTs have emerged as excellent devices for high frequency, high power as well as high temperature applications [1], [2]. This technology is progressing rapidly and production level optimized circuit design with GaN HEMTs need accurate, fast and efficient compact models. Available models [3–6] for GaN HEMTs range from empirical to physics-based models. However, surface-potential or charge-based model ensues better predictability and scalability due to their physical formulation. A very important advantage that physics based compact models have is that they are suitable for use in a wide field of application i.e a single model code can be used for RF as well as power electronic application.

In this paper, we present an overview of ASM-HEMT model, which is an analytical surface-potential based model and currently under standardization process at the CMC [7]. Several model features which are important for the modeling of high power or high frequency GaN HEMT, are highlighted. Finally the model is validated with the measured data of Toshiba (high power) and Qorvo (RF) GaN HEMTs.

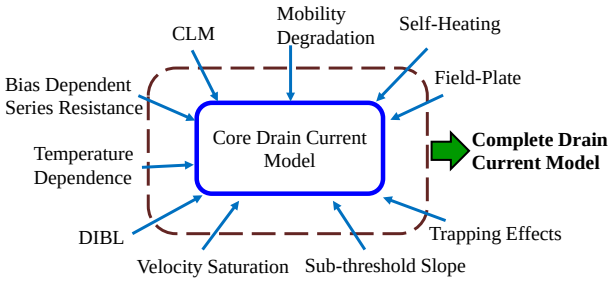


Fig. 1: Schematic of core drain-current model showing all the real device effects incorporated in ASM-HEMT model.

II. Model Description

In the following subsections, core model formulation to obtain drain current and terminal charges are briefly presented along with the recent enhancements to make the overall model compatible for use in wide range of applications.

A. Surface Potential and Terminal Charges

A closed form expression for unified Fermi level valid for the entire region of operation is obtained [8] by self-consistent solution of Schrodinger and Poisson equations in the AlGaN/GaN triangular potential well, considering the first two energy subbands. The unified Fermi level expression is given as [8]

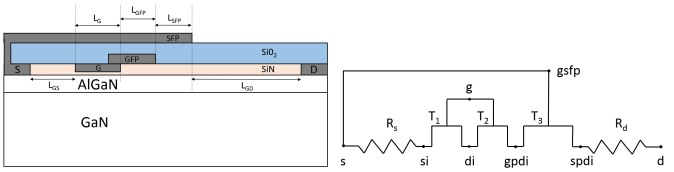
$$E_{f,unified} = V_{go} - \frac{2V_t ln\left(1 + e^{\frac{V_{go}}{2V_t}}\right)}{\frac{1}{H(V_{go,p})} + (C_g/qD)e^{-\frac{V_{go}}{2V_t}}} \quad (1)$$

where, C_g is the gate capacitance per unit area, q is the electronic charge, D is the density of states, $V_{go} = V_{gs} - V_{OFF}$, V_{OFF} is the cut-off voltage and V_t is the thermal voltage. Function $H(V_{go,p})$ captures the bias dependence of the Fermi level for $V_{go} > V_{OFF}$. The surface potential is obtained from the expression $\psi = E_f + V_x$, where V_x is the channel potential.

This surface potential formulation is used to calculate the terminal charges. The gate charge is obtained [8] by integrating the 2-DEG charge along the channel as follows:

$$Q_g = -\int_0^L qWndx = -\int_0^L qWC_g(V_{go} - \psi)dx \quad (2)$$

where n signifies the 2-DEG charge density. The source and drain charges are calculated using Ward-Dutton partitioning scheme [9].



(a) (b)

Fig. 2: Typical cross-sectional view of the dual FP device showing the gate and source FPs and their appropriate connections to gate and source respectively. T1, T2 and T3 denote Intrinsic, Gate FP and Source FP transistors respectively. The intrinsic nodes within the device are also indicated.

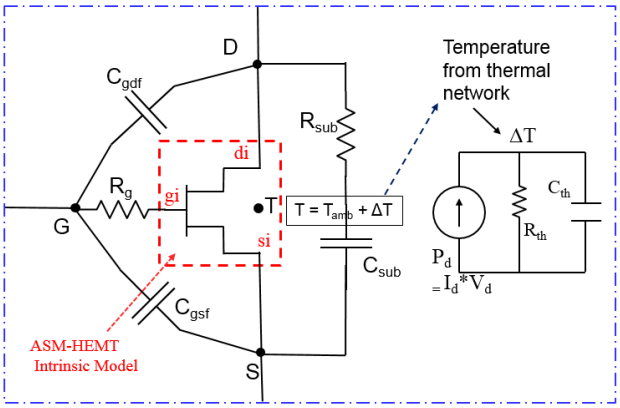


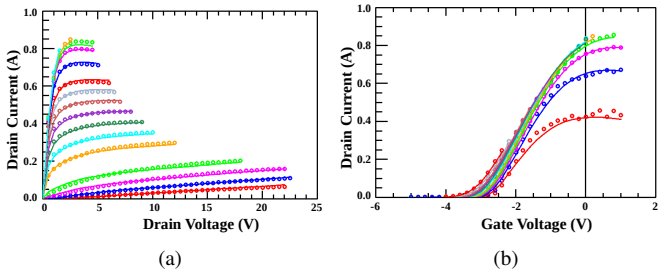
Fig. 3: Equivalent ASM-GaN-HEMT model showing parasitic elements. R_g models the gate-resistance effect. R_{sub} and C_{sub} model the substrate loss at RF. C_{gdf} and C_{gsf} are fringe capacitances. Self-heating is modeled with thermal network. The sub-circuit shown in blue dotted lines is combined with standard pad parasitic model for simulations.

B. Drain Current

The drain current is calculated using the surface potential formulation under drift-diffusion framework and given as [10]

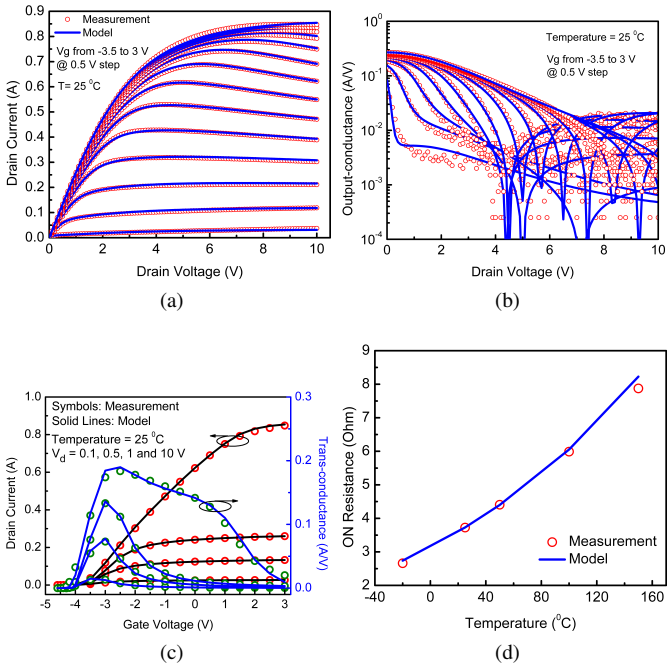
$$I_{ds} = \frac{\mu_{eff} C_g}{\sqrt{1+\theta_{sat}^2 \psi_{ds}^2}} \frac{W}{L} \left(V_{go} - \psi_m + V_{th}\right) \left(\psi_{ds}\right) \left(1 + \lambda V_{ds,eff}\right) \tag{3}$$

where $\psi_{ds} = \psi_d - \psi_s$ and $\psi_m = (\psi_d + \psi_s)/2$. The velocity saturation effect is included in (3) through the velocity saturation parameter θ_{sat} and the channel length modulation effect through λ. The mobility degradation due to the vertical field is also included in μ_{eff}. Accurate modeling of plethora of real device effects including DIBL, self-heating effect, temperature dependence, non-linear access region resistances etc. have been included in the complete I_d model to represent a realistic GaN HEMT device and is presented in Fig. 1.



(a) (b)

Fig. 4: (a) $I_d - V_d$ and (b) $I_d - V_g$ model comparison with measured data for Qorvo RF GaN HEMT ($W = 10 \times 90\mu m$, L_g =125nm); symbol (measurement) and solid line (model).



(a) (b) (c) (d)

Fig. 5: (a) $I_d - V_d$, (b) output-conductance (g_d) and (c) $I_d - V_g$ (left Y-axis), transconductance (g_m) (right Y-axis) for the Toshiba power GaN HEMT, showing the model's capability to capture the source/drain access region resistances at higher V_g; (d) variation of R_{ON} with temperature validating the temperature dependence of the model.

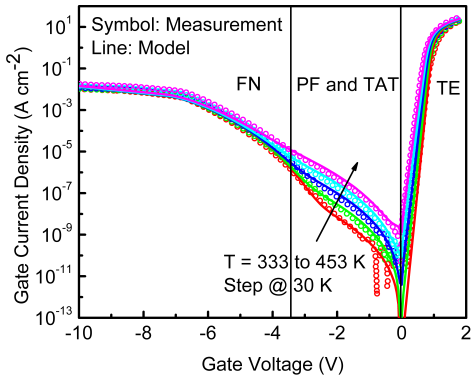
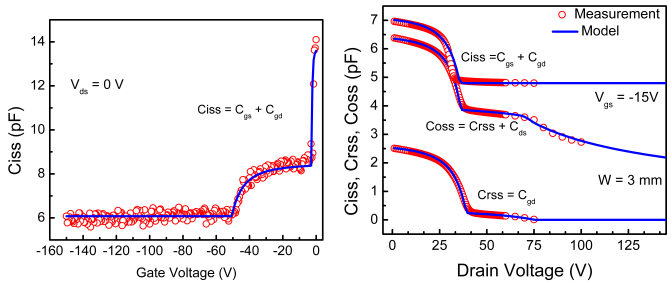


Fig. 6: Experimental gate current density data [13] and model for a wide range of temperatures (from 333 to 453 K with a step size of 30 K), showing the three bias regions. Weak temperature dependence in high reverse bias and strong temperature dependence at medium reverse bias clearly distinguish the FN and PF current components for this device (Al mole fraction 33 %); TE plays important role in forward bias region. Impact of the gate-resistance is seen in high forward bias region.

C. Source/Drain Access Region Resistance Model

In GaN HEMT, a short gate-to-source distance L_{gs} and optimized gate-to-drain distance L_{gd} are required as a trade-off between breakdown-voltage (BV) and transit frequency (f_t). This gate-to-drain/source access region works as non-linear resistance ($R_{d/s}$), which limits maximum drain current. Accurate modeling of the access resistance is very important to correctly predict the drain current, transconductance (g_m) and hence the f_T at higher current. A current dependent nonlinear source/drain access resistance model of AlGaN/GaN HEMTs



(a) (b)

Fig. 7: (a) Comparison of the modeled $Ciss - V_g$ with experimental data at $V_d = 0V$ for the Toshiba device; (b) variation of $Ciss$, $Crss$ and $Coss$ with V_d at sub-threshold condition ($V_g = -15V$).

is developed [11] and given as

$$R_{d/s} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}} \tag{4}$$

where $I_{acc,sat}$ is the saturation current or maximum current supported in the access region and low current access resistance $R_{d0/s0} = L_{acc}/(Q_{acc} \cdot \mu_{acc})$. We can observe that $R_{d/s}$ increases rapidly as I_d approaches to $I_{acc,sat}$ which limits the total drain current flowing through the device.

D. Gate Current

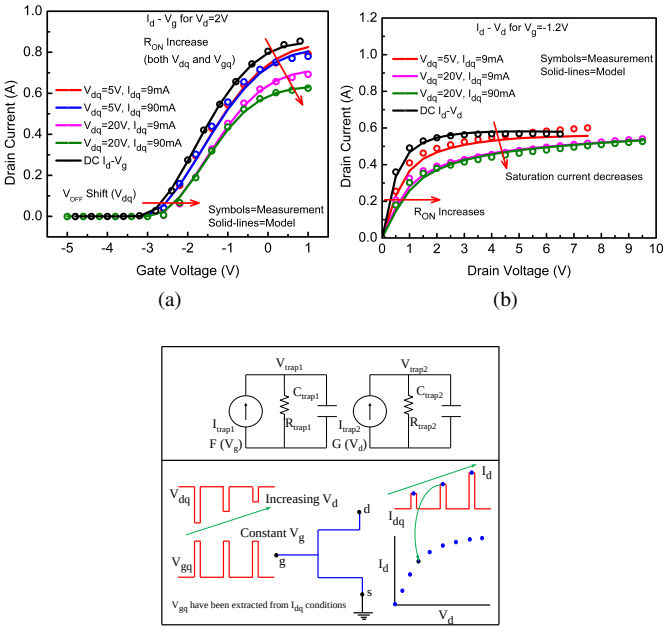
An analytical model for the gate leakage current (I_g) is developed [12] in a surface-potential based framework. The total gate current consists of Poole-Frenkel (PF) emission (medium to low reverse gate voltage), Thermionic emission (TE) (forward bias), trap-assisted tunneling (TAT) (closed to origin) and Fowler-Nordheim (FN) tunneling current (high reverse bias). The FN tunneling component has a significant impact in the GaN HEMT with higher Al mole fraction in the barrier layer [13].

E. Noise Models

Analytical models for low frequency flicker noise [14] and high frequency thermal noise [15] are also incorporated in ASM-HEMT. Both the carrier number fluctuation and mobility fluctuations are taken into account in the flicker noise model. The thermal noise model is based on the approach by Klaassen and Prins. The noise models also include the induced thermal noise due to gate-channel coupling [16].

F. Field-Plate Model

FP incorporation in GaN HEMT improves breakdown voltage, reduces gate leakage current and surface trapping effect, but it strongly affects the capacitance behavior of the device. Accurate modeling of FP capacitances is very important as it controls the switching characteristics of the device. A typical source and gate connected FP device is shown in Fig. 2(a). We have modeled [17] the FP regions as series connected transistors with the intrinsic one and shown in Fig. 2(b). The passivation and barrier materials in between FP and 2-DEG charge determine the cut-off voltage of these FP transistors. The charge and current models for these FP transistors are



(a) (b)

(c)

Fig. 8: DC and Pulsed (a) $I_d - V_g$ (b) $I_d - V_d$ for various V_{dq} and I_{dq} conditions; Model showing the good agreement with the experimental data for Qorvo device; (c) R-C subcircuits implemented in Verilog-A to model the trapping effect and simulation strategy (shown for pulsed $I_d - V_d$) in Keysight ICCAP software.

formulated in a similar manner given in sections A and B. Additionally the cross-coupling charges due to the fringing field are also included in the model.

G. Temperature Dependence

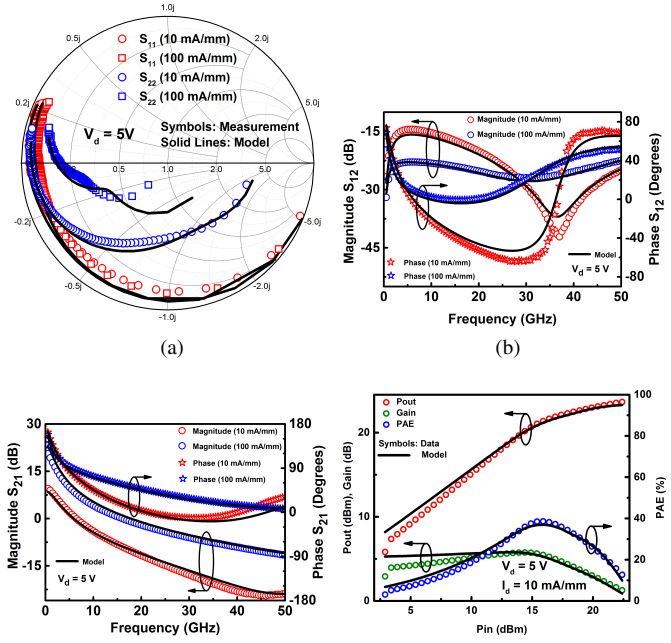
A temperature dependent model of AlGaN/GaN HEMTs is developed which can capture the temperature effects of 2-DEG electron mobility, threshold voltage, saturation velocity in the channel and source/drain access region. The temperature dependence of $R_{d/s}$ model is extremely important as it increases significantly with increasing temperature especially for the short channel devices [11]. The noise models, gate current and field-plate models are also temperature dependent.

H. RF Model

Accurate RF modeling needs models for parasitic capacitances and resistances in addition to the intrinsic terminal charges. At the input terminal, gate resistance becomes important at RF while at the output terminal, substrate losses need to be accounted for. These parasitic effects are accounted for in our model and complete model can be represented as shown in Fig. 3. Accurate modeling of small-signal RF (S-parameters) can be accomplished with model shown in Fig. 3. However, accurate large signal RF modeling needs model for trapping effects which is described in the next sub-section.

I. Modeling of Trapping Effects

Traps in GaN HEMTs play huge role in determining the performance of the device, especially in high frequency operations and hence incorporation of nonlinear trapping effect in the GaN HEMT compact model is very important. The



(a) (b) (c) (d)

Fig. 9: Accurate modeling of small-signal S-parameters for frequency range $500MHz$ to $50GHz$ at $V_d = 5V$ and two different current condtions $I_d = 10mA/mm$ and $100mA/mm$: (a) S_{11} and S_{22}; (b) magnitude (left Y-axis) and phase (right Y-axis) of S_{12}, and (c) magnitude (left Y-axis) and phase (right Y-axis) of S_{21}; (d) modeling of large-signal RF output power (P_{out}), RF power gain and PAE (%) as the input power P_{in} is varied while input signal frequency is $10GHz$; the trapping effects are included through the trap model.

pulsed I-V characterization is carried out to study the transient behavior of the device and in turn understand the physics of transient phenomenon like trapping and de-trapping of charges and the resulting effects in the current characteristics. The trapping effects are modeled with the help of two R-C sub-circuits [18]. The generated trap voltages V_{trap1} and V_{trap2} are fed back into the model which update parameters like the cut-off voltage, sub-threshold slope, source and drain-resistances to capture the effects of traps.

III. Results and Discussion

We have rigorously validated our model with experimental data for Toshiba's high power (gate and source connected dual FP structure) and Qorvo RF GaN HEMT ($W = 10 \times 90\mu m$) which was provided as a part of standardization activity at CMC. Good agreement between measured $I_d - V_d$ and $I_d - V_g$ with the model is shown in Fig. 4(a) and (b), respectively, for the Qorvo device. The effect of source/drain access region's resistance and the self heating effect are clearly observed and captured in Fig. 5(a), (b) and (c), at higher V_g for the Toshiba device. The temperature dependence of R_{on} is shown in Fig. 5(d). Weak and strong temperature dependence of FN and PF dominated regions, respectively, in the total gate current are presented in Fig. 6.

The effect of gate and source connected FPs in the capacitance behavior for the Toshiba device is accurately captured by the model and is presented in Fig. 7(a), (b). In the $Ciss - V_g$ plot (Fig. 7(a)), the first hump is due the intrinsic transistor ($V_{off} = -2.3V$) whereas, the second hump is appearing due to the gate FP ($V_{off} = -50.5V$). The off-state capacitances (Ciss, Crss and Coss) with V_d in Fig. 7(b) are only due to the gate and source FP charges and their cross coupling effect due to the fringing fields.

Before going to the RF parameter extraction part, we extracted the trap model parameters and the results are shown in Fig. 8(a) and (b) for the Qorvo device. Threshold voltage shift and increase of R_{ON} are accurately modeled for different quiescent drain bias and current conditions in the dual pulsed measurement. The R-C sub-circuits implemented in the Verilog-A code and the simulation strategy for the pulsed $I-V$ are shown in Fig. 8(c).

In Fig. 9(a), (b) and (c), we show model results for S-parameters measured from 500 MHz to 50 GHz at two DC bias points. Accurate modeling of S-parameters shows that non-linear behavior of g_m, g_d and capacitances is accurately modeled. Large signal RF results starting with the RF input power sweep characteristics are shown in Fig. 9(d). We show the variation in output power Pout, Power Gain, and Power-added efficiency (PAE) for $V_d = 5V$ and $I_d = 10mA/mm$ condition in Fig. 9(d). Accurate modeling of these key figures has been achieved with the help of physics based core and trapping effects model.

IV. Conclusion

We have presented an overview of accurate and analytical surface potential based GaN HEMT model. The model has been validated for two devices (high power and high frequency GaN HEMTs) and shows good match with the measurement. The Verilog-A implemented model has been validated on different commercial simulators for wide temperature and bias ranges, which signifies the computational efficiency and robustness of the model.

Acknowledgment

This work was partially funded by DST Fast Track Scheme for Young Scientists, ISRO, CSIR, and Ramanujan Fellowship. We would like to thank Toshiba Corporation and Qorvo for providing measurement data as a part of Si2-CMC model standardization activity.

References

[1] R. Rupp et al., *IEEE IEDM* 2014 pp. 2.3.1-2.3.4.
[2] U. K. Mishra et al., *Proc. IEEE*, vol. 96, no. 2, pp. 287-305, Feb. 2008.
[3] I. Angelov et al., *IEEE MTT*, vol. 40, no. 12, pp. 2258-66, 1992.
[4] O. Jardel et al. *IEEE MTT*, vol. 55, no. 12, pp. 2660-69, 2007.
[5] U. Radhakrishna et al., *IEEE IEDM* 2014, pp. 11.6.1 11.6.4.
[6] S. Khandelwal et al., *IEEE TED*, vol. 58, no. 10, pp. 3622-25, 2011.
[7] S. D. Mertens, *IEEE CSICS*, pp. 1-4, 19-22 Oct. 2014.
[8] S. Khandelwal et al., *IEEE TED*, vol.59, no.10, pp.2856-2860, Oct. 2012.
[9] S. Oh et. al., *IEEE SSC*, Aug. 1980.
[10] S. Khandelwal et al., *SSE*, vol 76, pp. 60-66, Oct. 2012.
[11] S. Ghosh et al., *IEEE EDSSC*, pp. 1-4, Aug. 2016.
[12] S. Ghosh et al., *IEEE TED*, vol. 62, no. 2, pp. 443-448, Feb. 2015.
[13] S. Turuvekere et al., *IEEE TED*, vol. 61, no. 12, pp. 4291-4294, Dec. 2014.
[14] A. Dasgupta et al., *IEEE JEDS*, Vol. 2, no. 6, pp. 174-178, 2014.
[15] A. Dasgupta et al., *IEEE MWCL*, Vol. 25, no. 6, pp. 376-378, 2015.
[16] A. Dasgupta et al., *IEEE MWCL*, Vol. 26, no. 6, pp. 428-430, 2016.
[17] S. A. Ahsan et al., *IEEE TED*, Vol. 63, no. 2, pp. 565-572, 2016.
[18] S. Ghosh et al., *IWPSD*, Dec. 2015.