Analysis and Modeling of Cross-Coupling and Substrate Capacitances in GaN HEMTs for Power-Electronic Applications

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***Abstract*— In this paper, we present a capacitance model for field-plate AlGaN/GaN High Electron Mobility Transistor (HEMTs) accounting for the contribution of substrate capacitances and cross-coupling between field plates. TCAD simulations are performed to analyze both these contributions and analytical expressions for charges corresponding to the cross-coupling and substrate capacitances are presented in terms of our existing surface-potential-based model. The modeled results are validated by comparing the time-domain waveforms of a test circuit using a mixed-mode simulation setup in which the impact of cross-coupling and substrate capacitances on accuracy of switching transients predicted by the model is discussed.**

***Index Terms*— Capacitance, cross-coupling, GaN HEMTs, mixed-mode, substrate, switching.**

I. Introduction

UNTIL the very beginning of the 21st century, the high power industry was dominated by devices based on silicon (Si); however, their performance improvement is proving very difficult because of limitations in material properties of Si. Material systems based on wide bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), offer great advantages over their Si-based counterparts [1], [2]. GaN FETs are promising to be the workhorse of the future power-electronic and power-management industry, owing to the excellent material properties of the GaN [3]–[6], such as high values of low field mobility, saturation velocity, breakdown electric field, and so on, to name a few. As a result, the Baliga figure of merit [7], which is a benchmark metric of performance for power devices, is highly superior for GaN High Electron Mobility Transistor (HEMTs) [3].

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In order to push the breakdown voltages of these GaN-based devices further toward the higher side, a lot of device structure tailoring has happened over the years in terms of field plate (FP) incorporation, such as air-bridges [8], slant FPs [9], multiple FPs [10], [11], and so on. These evolved structures lead to complexities in the capacitance behavior which may significantly affect the switching performance of these devices. For production level tape-out of power electronic circuits based on advanced power GaN FP structures, there is an immediate need for an efficient and accurate compact model for GaN HEMTs.

Existing literature reports about studies carried out on FP capacitances and their modeling in GaN devices; however, a fully physics-based model without making any compromise on the accuracy is still a hot topic of research [12], [13]. Curve-fitting with datasheet [14], [15] and lookup table-based [16] methods is already reported to evaluate the terminal capacitances. Cucak *et al.* [17] presented a physics-based analytical model; however, it is significantly inaccurate in predicting the cutoff voltage for the FP while compromising on fitting the capacitance plateaus with measured data. We recently proposed a physics-based FP capacitance model for GaN HEMTs, which has a surface-potential calculation at its core and validated it against measured data for a commercial power GaN HEMT [18]. The model is currently in the final stage of evaluation for getting standardized by the compact model coalition [19], [20], [22]–[24]. In this paper, we aim to extend our model, and include cross-coupling and substrate capacitances, supplemented with further analysis on various aspects of GaN FP capacitances using TCAD and mixed-mode simulations.

This paper is organized as follows. Section II describes the origin of cross-coupling and substrate capacitances for the FP GaN HEMT using TCAD. The approach followed to model those effects is discussed in Section III. Validation of the model with demo-circuit time-domain waveforms is done in Section IV. Finally, this paper is concluded in Section V.

II. Cross-Coupling and Substrate Capacitances—TCAD Analysis

A. TCAD Simulation Setup

Fig. 1 shows the TCAD representation of the AlGaN/GaN FP device performed in Silvaco Atlas [25]. Standard FP

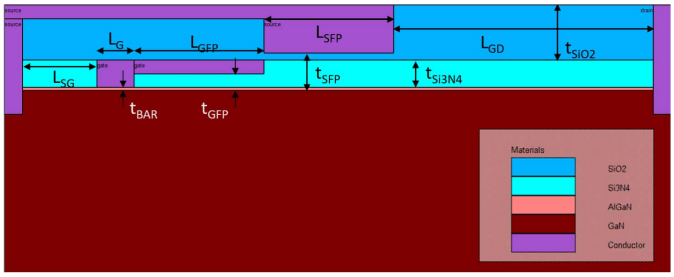

Fig. 1. Cross-sectional view of the GaN HEMT dual-FP structure simulated in Silvaco Atlas. The structure dimensions are $L_G = 1\ \mu$m, $W = 3$ mm, $L_{GFP} = L_{SFP} = 3.5\ \mu$m, $L_{SG} = 2\ \mu$m, $L_{GD} = 7\ \mu$m, $t_{BAR} = 20$ nm, $t_{GFP} = 120$ nm, and $t_{SFP} = 270$ nm. Effective oxide thickness values for t_{GFP} and t_{SFP} with respect to t_{BAR} are evaluated and used in the model.

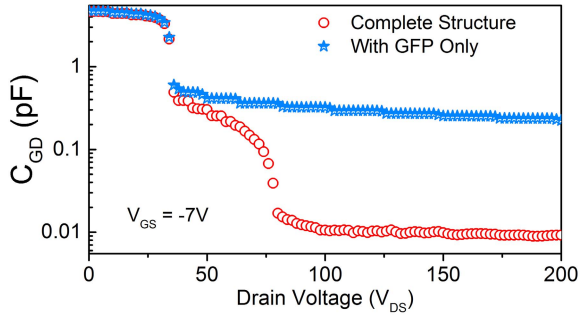

Fig. 2. Comparison of the simulated subthreshold C_{gd} for dual-FP and GFP-only structures. The absence of the second plateau for single FP structure highlights the cross-coupling phenomenon. V_{gs} is fixed at -7 V, while V_{ds} is swept from 0 to 200 V.

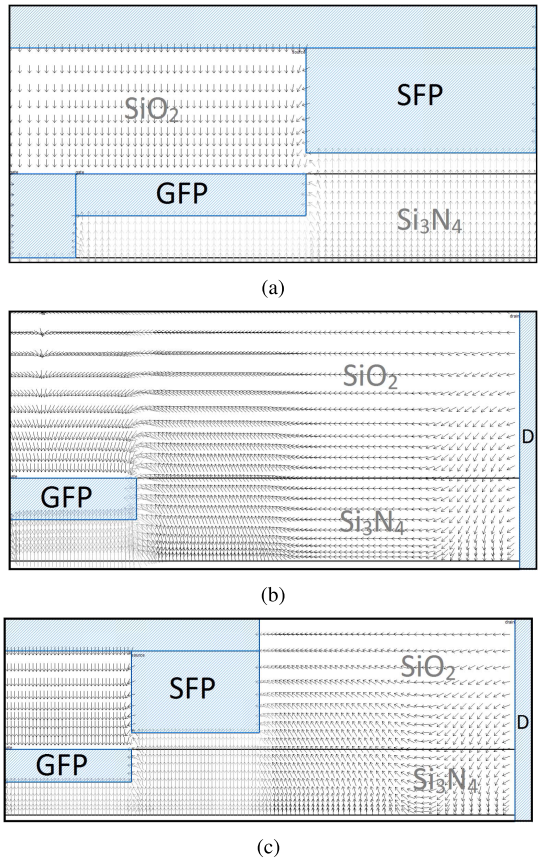

Fig. 3. Vector plots of electric field lines for $V_{gs} = -7$ V. (a) $V_{ds} = 40$ V. The appearance of fringing electric field between the vertical wall of the GFP and the 2-DEG$_{SFP}$ causes the cross-coupling effect giving rise to the second plateau in Fig. 2. Vector plots of electric field lines for $V_{gs} = -7$ V and $V_{ds} = 100$ V. (b) Significant number of fringing field lines reach the GFP through the insulator stack. (c) In the presence of the SFP, most of them end up at the SFP leading to a reduced fringing capacitance component in C_{gd}. The varying gray scale of the vector plots represents an electric field magnitude of 3.6×10^6 V/cm (gray) to 2.68×10^5 V/cm (black).

topology of having a gate-connected (GFP) and a source-connected (SFP) field-plate is considered. Spontaneous polarization charges are added to the top and bottom surfaces of both the AlGaN and GaN layers through the polarization models. Piezoelectric charge is calculated separately by the strain model based on the lattice mismatch between AlGaN and GaN by having a value of 0.25 for the Al mole-fraction in the AlGaN layer. A self-consistent solution of the Poisson equation and continuity equations is obtained numerically by Altas while incorporating the physical models. Albrecht's Model [26] for bulk mobility is used while field-dependent mobility model [27] is also used to account for the saturation of carrier velocity at high lateral fields.

B. Cross-Coupling Capacitance

It is well known that the incorporation of GFP significantly increases the reverse Miller capacitance (C_{gd}), whereas SFP introduces an additional drain–source capacitance (C_{ds}) in the form of plateau-like features [3]. However, in advanced GaN FP structures, multiple capacitance plateaus are seen [28], and the explanation for which is given as follows.

The TCAD simulated subthreshold ($V_{gs} < V_{OFF}$) C_{gd} plots for the device with both FPs as well as for the GFP-only structure is shown in Fig. 2. For the device with both GFP and SFP, the first plateau in C_{gd} corresponds to the progressive extension of depletion region, under the influence of the GFP, toward the drain with increasing V_{ds}, until full depletion of the 2-D electron gas (2-DEG) under the GFP occurs. The second plateau appears due to the cross-coupling influence of the GFP on the 2-DEG under the SFP (2-DEG$_{SFP}$). It can be better understood by observing C_{gd} for the GFP-only structure, where the second plateau feature seems to be missing, clearly indicating the cross-coupling effect of the GFP on 2-DEG$_{SFP}$ in the previous case. Further support to this argument is added by the field lines emanating from the GFP and terminating at the 2-DEG$_{SFP}$, shown in Fig. 3(a). One might argue that fringing field lines would still exist between the GFP and the adjacent 2-DEG in the drain access region even in the absence of SFP, which might still lead to some sort of capacitance plateau. However, it is a point worth noting that the access region charge in that case is different from the 2-DEG$_{SFP}$ which has a different bias-dependence profile, a different cutoff voltage and is controlled by its own independent gate, which is the SFP. This is what differentiates the usual depletion-type capacitance for the GFP-only device from the plateau-shaped cross-coupling capacitance in C_{gd}.

The bias-independent parasitic value of C_{gd}, which is due to the fringing field between the drain-electrode and the GFP,

increases for the GFP-only structure in comparison with the structure with both FPs. It is because of a significant number of fringing field lines reaching the GFP through the insulator stack, whereas in presence of the SFP, most of them end up at the SFP leading to a reduced fringing capacitance component in C_{gd}, as shown in Fig. 3(b) and (c).

C. Substrate Capacitance

The introduction of a substrate electrode introduces a capacitance between the substrate and the other three intrinsic device nodes, namely, the gate, drain, and source where the GaN buffer acts as a dielectric. The substrate-drain capacitance (C_{SUBD}), however, needs more attention since it forms a part of the overall output terminal capacitance (C_{OSS}). As shown in Fig. 4, a lot of field lines originating from the 2-DEG reach the substrate electrode [see Fig. 4(a)], whereas in its absence, field lines from the drain side of the 2-DEG terminate at the 2-DEG on the source side through the GaN buffer [see Fig. 4(b)]. In Fig. 6, as can be observed, C_{SUBD} manifests a double-plateau behavior similar to that of C_{gd} with each plateau appearing for bias conditions at which some significant 2-DEG exists beneath the corresponding FP. It essentially suggests a similarity between the 2-DEG and the associated substrate charge toward changing gate and drain biases—an approach that we later follow to model C_{SUBD}.

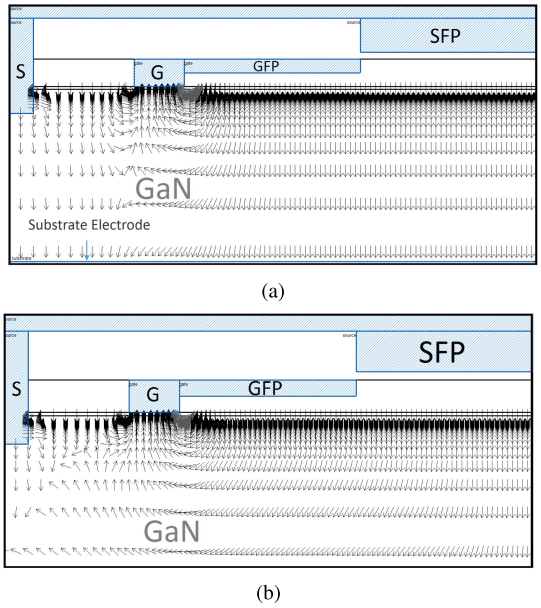

Fig. 4. Vector plots of electric field lines for $V_{gs} = -7$ V and $V_{ds} = 20$ V. Field lines originating from the 2-DEG reach the substrate electrode [see (a)] leading to the existence of C_{SUBD}, whereas in its absence, field lines from the drain side of the 2-DEG terminate at the 2-DEG on the source side through the GaN buffer [see (b)]. The varying gray scale of the vector plots represents an electric field magnitude of 1.32×10^6 V/cm (gray) to 1.09×10^5 V/cm (black).

III. Cross-Coupling and Substrate Capacitances—Modeling

In our previous work, we evaluated the intrinsic device charges as well as the drain current in terms of the surface-potential (ψ). Further details on ψ calculations and the overall FET I-V model can be found in [20]–[22]. We calculated the intrinsic capacitances of the FP device by modeling each FP as a separate transistor with its own set of calculations [18]. Here, we follow the similar procedure to compute the cross-coupling and substrate capacitances in terms of ψ.

As discussed in Section II, the GFP modulates some part of the 2-DEG lying beneath the SFP, leading to some finite amount of cross-coupling charges given in (1), as shown at the bottom of this page, where Q_{cc} represents the cross-coupling charge between the GFP and the 2-DEG$_{SFP}$. α_{cc} denotes a dimensionless scaling factor that determines the strength of cross-coupling effect. The details on various symbols used in the expressions can be found in [18].

The cross-coupling capacitance can now be evaluated by assigning this charge between the gate of the GFP transistor and source of the SFP transistor, as under

$$C_{GFP-SFP} = -\frac{dQ_{cc}}{dV_{s,SFP}}. \tag{4}$$

$C_{GFP-SFP}$ is added to C_{gd} leading to the double-plateau features, as shown in Fig. 5, where the comparison between the model and the TCAD results is made.

In order to model the substrate capacitances, we associate some charges to the substrate node and divide it into

$$Q_{cc} = -\alpha_{cc} \times WL_{SFP}C_{g,SFP}\left\{V_{go,SFP} - \frac{1}{2}(\psi_{s,SFP} + \psi_{d,SFP}) + \frac{(\psi_{d,SFP} - \psi_{s,SFP})^2}{12\left(V_{go,SFP} - \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,SFP} + \psi_{d,SFP})\right)^2}\right\} \tag{1}$$

$$Q_{SUB,k} = -\beta_k \times WL_kC_{g,k}\left\{V_{go,k} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k}) + \frac{(\psi_{d,k} - \psi_{s,k})^2}{12\left(V_{go,k} - \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k})\right)^2}\right\} \tag{2}$$

$$Q_{d,SUB,k} = -\beta_k \times \frac{1}{2}WL_kC_{g,k}\left\{V_{go,k} - \frac{1}{3}(\psi_{s,k} + 2\psi_{d,k}) + \frac{1}{12}\left(\frac{\psi_{ds,k}^2}{\left(V_{go,k} + \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k})\right)}\right) + \frac{1}{12}\psi_{ds,k}^3\left(V_{go,k} + \frac{K_BT}{q} - \frac{1}{2}(\psi_{s,k} + \psi_{d,k})\right)^2\right\} \tag{3}$$

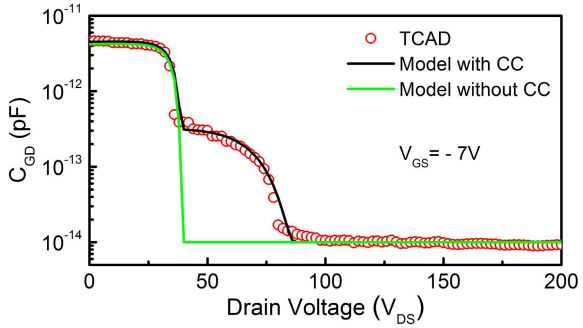

Fig. 5. Comparison of the modeled C_{gd}, with TCAD data under subthreshold conditions for GaN FP HEMT. Model without cross-coupling capacitances is also shown in which the second plateau is seen missing. V_{gs} is fixed at -7 V, while V_{ds} is swept from 0 to 200 V.

the regional substrate charges corresponding to the intrinsic transistor ($Q_{\mathrm{SUB},1}$), GFP ($Q_{\mathrm{SUB},2}$), and SFP ($Q_{\mathrm{SUB},3}$). Each one of these quantities is basically a scaled value of the 2-DEG for each transistor controlled by its own gate. So, effectively we model the substrate as a back-field-plate, with the GaN layer as the dielectric, which to some extent modulates the channel 2-DEG. The regional substrate charges are evaluated using the charge formulations of respective gate charges given in (2), as shown at the bottom of the previous page. In order to maintain charge neutrality within the substrate, drain, and source nodes of the device, we assign proportionally scaled charges to the drain and source nodes using existing formulations [18]. The drain charge is given in (3), as shown at the bottom of the previous page, where k is 1, 2, and 3 for intrinsic transistor, GFP, and SFP, respectively. β_k is a dimensionless scaling factor.

Charge conservation maintained between the substrate, drain, and source terminals allows us to obtain the source charge using (2) and (3) as

$$Q_{s,\mathrm{SUB},k} = -Q_{\mathrm{SUB},k} - Q_{d,\mathrm{SUB},k} \tag{5}$$

which ensures that no convergence issues are faced during SPICE simulation, making the model more robust.

Substrate capacitance can now be calculated as

$$C_{mn=\pm(dQ_m/dV_n)} \tag{6}$$

where $\pm$ is $+$ for $m = n$ and $-$ for $m \neq n$. Strong correlation is obtained between the modeled and TCAD results as shown in Fig. 6.

Due to the physics-based nature of the model, it exhibits a geometrical scalability feature, as shown in Fig. 7, where modeled capacitance simulations and their comparisons with TCAD data are demonstrated for various lengths of FPs (L_{GFP}, L_{SFP}) and insulator thicknesses (t_{SiO2}, t_{Si3N4}).

IV. Mixed-Mode Simulation Setup

Mixed-mode simulations are a combination of device and SPICE circuit simulations in which a numerical device model based on physical models is first generated and then put in an SPICE circuit netlist to study its behavior under specific operating conditions. Mixed-mode is a powerful tool to do a thorough examination of the device internal dynamics at

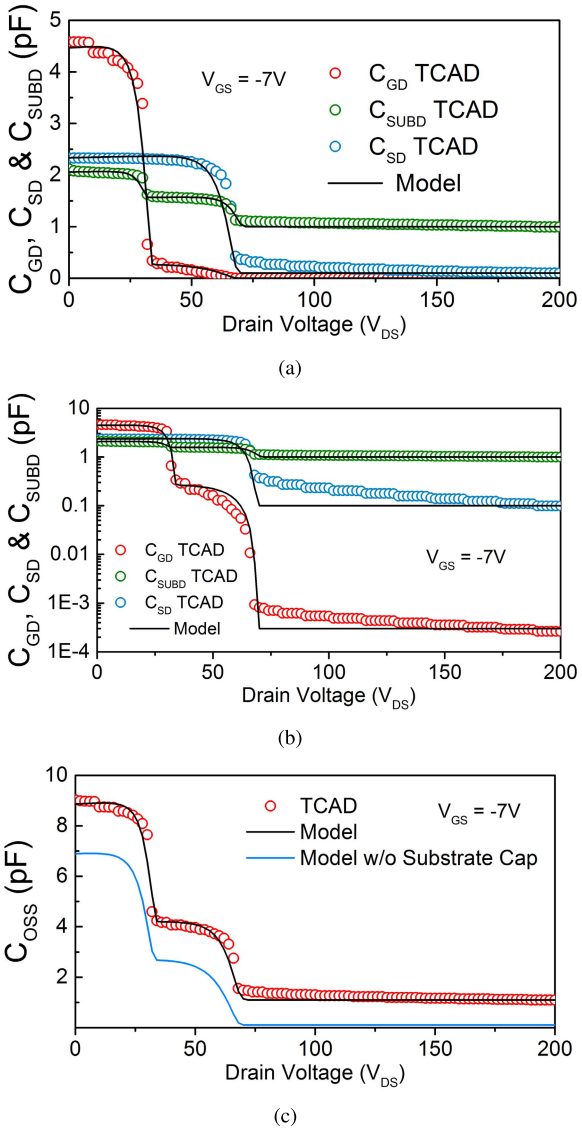

Fig. 6. Comparison of the modeled C_{gd}, C_{sd}, and C_{SUBD} with TCAD data under subthreshold conditions for GaN FP HEMT with substrate electrode. (a) Linear scale. (b) Logarithmic scale. (c) Comparison of the modeled $C_{\mathrm{OSS}} = C_{\mathrm{gd}} + C_{\mathrm{sd}} + C_{\mathrm{SUBD}}$ with TCAD data capturing precisely the contribution of C_{SUBD}.

particular instants of time, thereby making the task of device as well as circuit optimization significantly easier and inexpensive [29].

The Atlas device discussed in Section II is added to the SPICE circuit in Silvaco's mixed-mode utility. As shown in Fig. 8, the schematic for a switching demo-circuit is constructed having a typical inductive load, such as in the the case of motors, drives, and so on. Two-level Newton's algorithm is used to numerically solve the circuit and device equations in which a new set of contact voltages for the numerical device is provided by the solution of circuit equations [30]. The device simulator in turn performs the calculation of currents for the numerical device.

We would like to mention that all the model simulations performed in this paper have been carried out at room temperature ($T = 300$ K) and the impact of self-heating effect

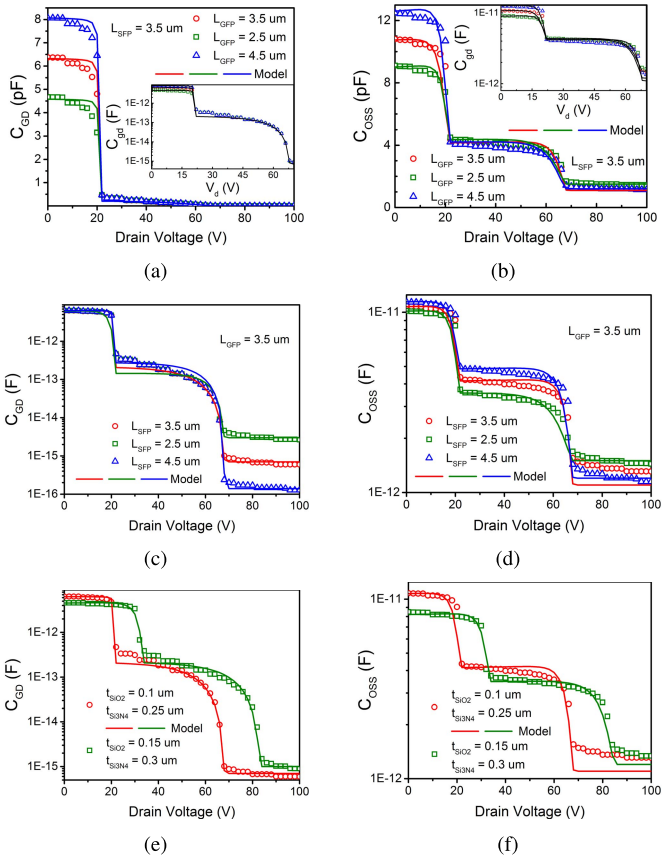

Fig. 7. Comparison of the modeled C_{gd} and C_{OSS} with TCAD data under subthreshold conditions for GaN FP HEMTs with a different (a) and (b) L_{GFP}, (c) and (d) L_{SFP}, and (e) and (f) t_{SiO2} and t_{Si3N4}. Excellent correlation is obtained between the TCAD and model simulations, therefore, highlighting scalability feature of the proposed model. Symbols: TCAD. Lines: model.

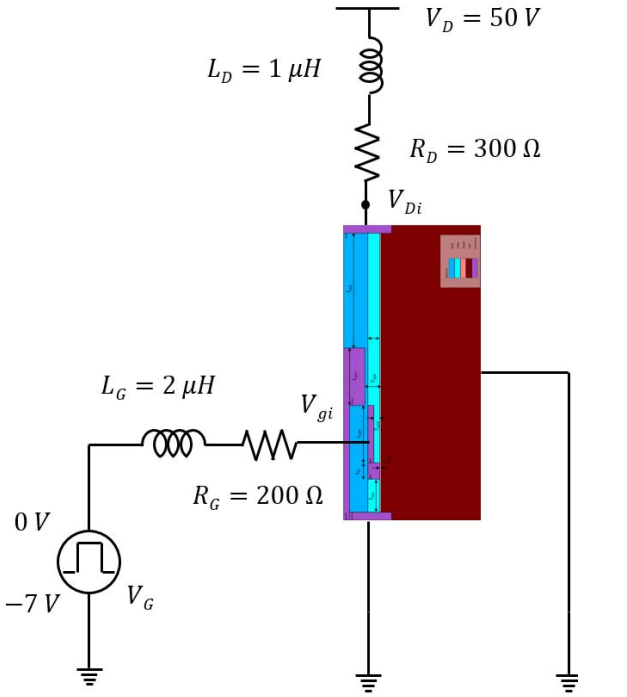

Fig. 8. Schematic for mixed-mode simulation using the numerical GaN FP device generated in atlas. The FP HEMT is put as the DUT with −7 and 0 V pulses of 1 MHz at gate. The pulse has a pulsewidth of 480 ns and 20 ns rise and fall times. Supply voltage of 50 V is chosen to capture the maximum effect of cross-coupling capacitances on switching transients, while an inductive load is put at the drain.

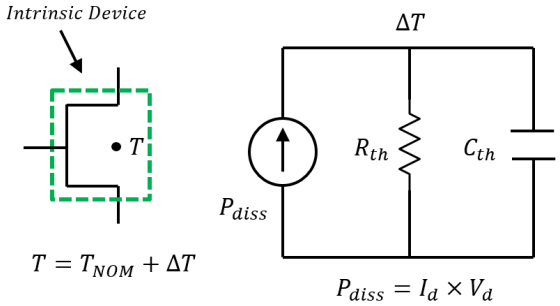

Fig. 9. *R–C* thermal network used to model the self-heating effect. The value of ΔT generated, which is a function of the dissipated power, is fed back into the compact model to update the operating temperature.

is captured by using a single pole RC thermal subcircuit, as shown in Fig. 9. The thermal node voltage generated, which is a function of the dissipated power ($I_d \times V_d$), gives the rise in temperature (ΔT) which is added to nominal temperature ($T_{\rm NOM}$).

A. Switching Transients

Transient simulations are carried out by applying a 1-MHz pulse, with a pulsewidth of 480 and 20 ns of rise and fall times at the extrinsic gate. Time-domain waveforms for intrinsic gate ($V_{\rm gi}$) and drain voltages ($V_{\rm di}$) and drain current (I_d) are obtained during turn-ON and turn-OFF. Subsequently, we extract the model card for the TCAD device from the $I_d - V_g$, $I_d - V_d$, and $C - V$ data using the parameter extraction procedure described in [31]. The same SPICE netlist is used for transient circuit simulation using the model in Keysight's ADS simulator [32] with the same operating conditions as in the mixed-mode netlist. The mixed-mode simulation for a time sweep of 1500 μs was completed in nearly 3000 s using a core-i7 3.4 GHz processor [33], whereas the SPICE simulation using our proposed compact model took 0.65 s using Intel Xeon E5 − 2690 2.9 GHz processor [33].

Fig. 10 shows the overlay plots for time-domain voltage and current waveforms extracted using mixed-mode and model simulations. During turn-ON, the gate drive current ($I_{\rm gg}$), given as

$$I_{\rm gg} = \frac{d}{dt}(C_{\rm gs}V_{\rm gs} + C_{\rm gd}V_{\rm gd}) \tag{7}$$

charges the gate node to the applied gate voltage ($V_{\rm gg}$) following the standard exponential behavior given by:

$$V_{\rm gs} = V_{\rm gg}\left(1 - e^{-\frac{t}{R_g(C_{\rm gs}+C_{\rm gd})}}\right) \tag{8}$$

until it reaches the cutoff voltage $V_{\rm OFF}$ during interval t_1. Until this point, most of the drive current goes into charging $C_{\rm gs}$ since it is much larger than $C_{\rm gd}$. After $V_{\rm gs}$ crosses $V_{\rm OFF}$, drain current starts to increase, causing V_d to decrease rapidly. Since $C_{\rm gd}$ is a strongly decreasing function of $V_{\rm ds}$, and $V_{\rm gd}$

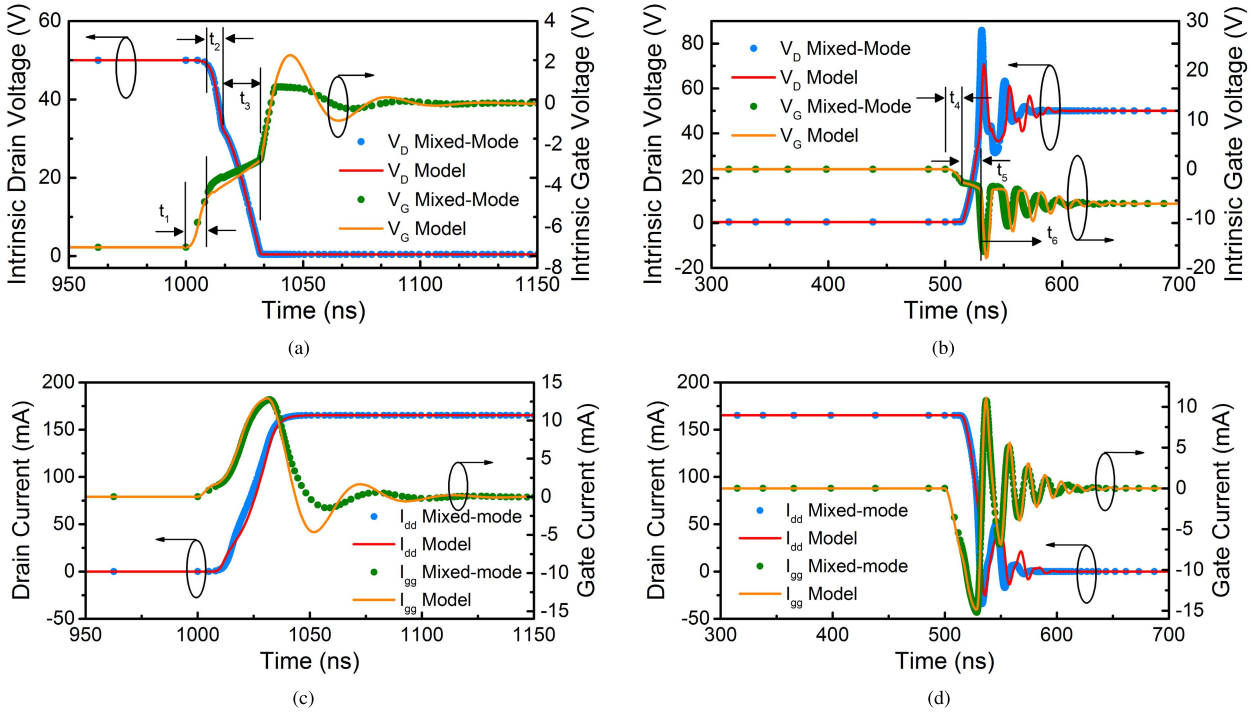

Fig. 10. Comparison of modeled time-domain waveforms for intrinsic drain voltage, gate voltage, and drain current with mixed-mode simulations during turn-ON and turn-OFF. (a) and (c) Turn-ON by switching applied gate signal from −7 to 0 V and (b) and (d) turn-OFF by switching applied gate signal from 0 to −7 V, keeping applied drain voltage fixed at 50 V. Model accurately predicts drain overshoots due to *LC* ringing, Miller plateaus due to accurate prediction in sharing of the gate drive current to charge C_{gs} and C_{gd} and the associated gate–drain charge, and the damping of the oscillations.

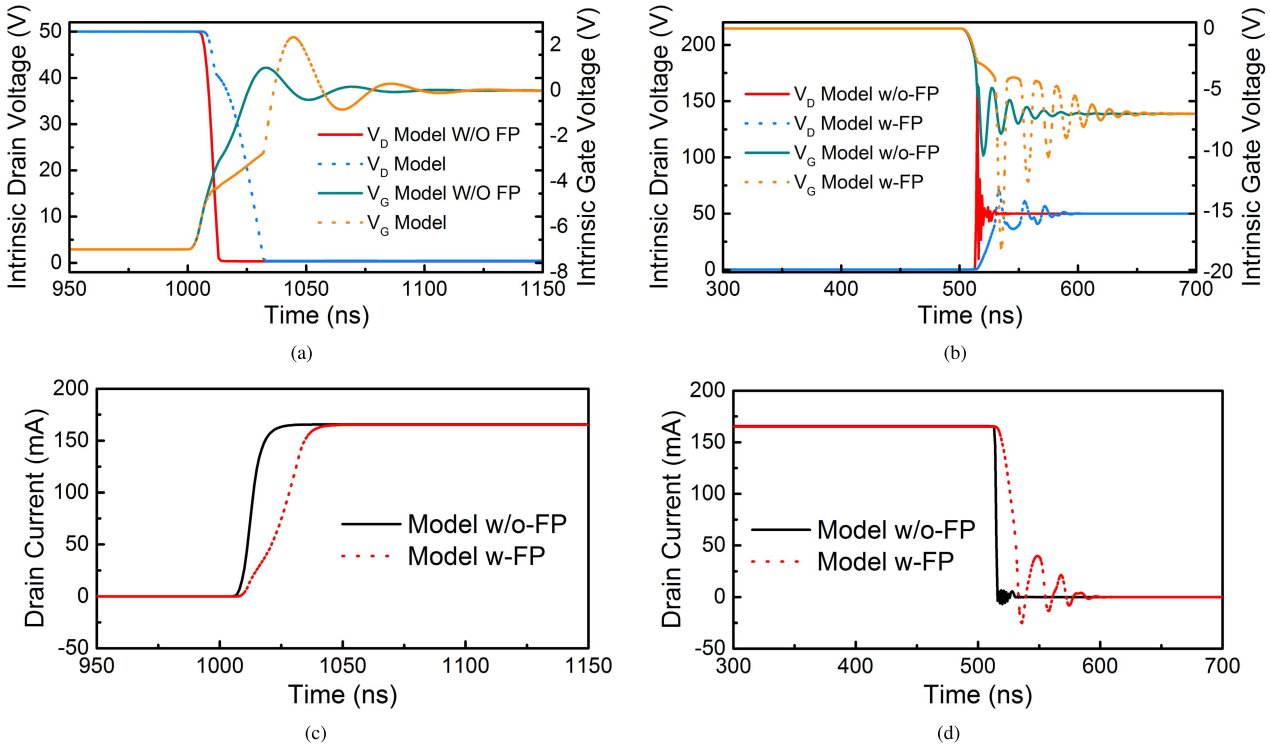

Fig. 11. Comparison of modeled time-domain waveforms during turn-ON and turn-OFF with and without improved FP Model. (a) and (c) Turn-ON by switching applied gate signal from −7 to 0 V and (b) and (d) turn-OFF by switching applied gate signal from 0 V to −7 V, keeping applied drain voltage fixed at 50 V. Significant difference in the slew rate as well as ringing of current and voltage waveforms is observed by including the FP model.

increases as V_{ds} decreases for a fixed V_{gs}, the derivative of $C_{gd}V_{gd}$ in (7) becomes significant, causing majority of I_{gg} to charge C_{gd} while keeping V_{gs} more or less fixed. This is known as the Miller plateau and goes on until the end of interval $t_2 + t_3$, where V_{ds} becomes a constant. We observe a nonzero slope in the Miller plateau, which can be ascribed to

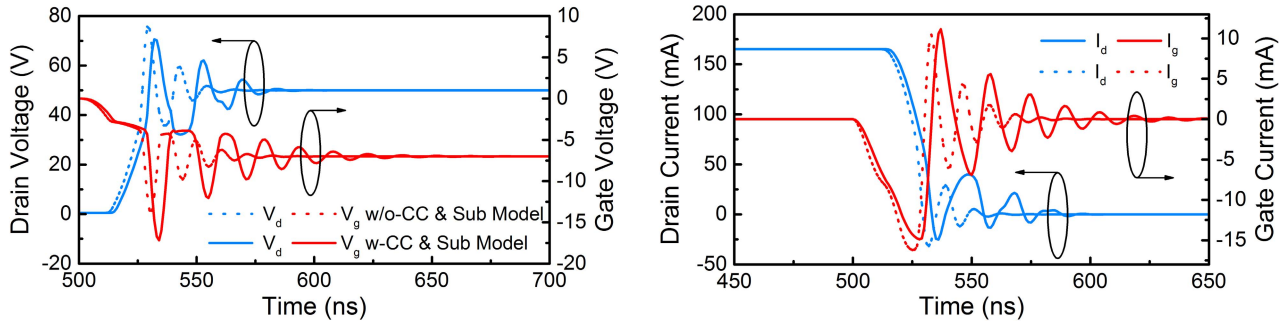

Fig. 12. Comparison of modeled time-domain waveforms during turn-OFF with and without cross-coupling and substrate capacitances. Even though the differences may not seem as much as observed in Fig. 11, however, from a power-electronics application point of view, differences in slew rates of 25%–30% as well as 10–15 ns of difference in settling times of waveforms is significant.

some fraction of I_{gg} charging C_{gs}. Beyond the Miller plateau, the device is fully ON and V_{gs} continues to rise following (8) although with a different time-constant due to higher values for C_{gs} and C_{gd}. Ringing due to LC-oscillations between L_g and input capacitances is also visible beyond t_3.

As far as the turn-OFF transients are concerned, V_{gs} in the interval t_4 decreases exponentially from an initial value of V_{gg}, with discharging time-constant corresponding to plateaued values of C_{gs} and C_{gd} since V_{ds} has an initial value of nearly 0 V. It represents the discharging of the input capacitance, while the current remains unchanged. A nonzero slope Miller plateau, similar to that observed while turn-ON, is observed during interval t_5, in which the drain current decreases while C_{gd} keeps discharging. It is during the same interval that the output capacitance C_{OSS} gets charged while current drops abruptly. Now that the device is fully OFF, in interval t_6, and due to the presence of an inductive load at the drain, which has an intrinsic tendency to oppose any abrupt change in current, the stored inductive energy gets converted into electrical energy in the form of very high voltage developed at the drain, leading to inductive spikes.

B. Impact of FP Model Including Cross-Coupling and Substrate Capacitances

Model predictions are sufficiently accurate to estimate transient characteristics such as the drain overshoots due to LC ringing [see Figs. 10(b) and 11(b)], Miller plateaus due to accurate prediction in sharing of the gate drive current to charge C_{gs} and C_{gd} [see Figs. 10(a) and 11(a)] and the associated gate–drain charge, and the damping of the oscillations [see Figs. 10(d) and 11(d)] in comparison with those predicted by mixed-mode simulations. A comparison of the transient waveforms during turn-OFF with and without the improved FP model is shown in Fig. 11, which shows the significance of the FP model. V_d was set to 50 V in the simulation to ensure that the excursions in V_{di} sweep the bias range for which impact of cross-coupling and substrate capacitances would be noticeable.

To understand the significance of the cross-coupling and substrate capacitances, in particular, turn-OFF transients simulated with and without the cross-coupling and substrate capacitances in the model are shown in Fig. 12. It represents different rates of charging of C_{OSS}. Due to the different values of C_{OSS} in both the cases, the slew rate as well as the extent of overshoots and their damping is noticeably different for intrinsic voltages and currents at the drain and gate nodes, therefore necessitating the inclusion of cross-coupling and substrate capacitances in the overall FP model for GaN HEMTs.

V. Conclusion

We presented an improved physics-based model for FP GaN HEMTs with regard to capacitances due to cross-coupling phenomenon and the substrate electrode. Thorough examination of these two features was performed using TCAD simulations. Appropriate mathematical expressions were presented to account for charges associated with cross-coupling and substrate electrode capacitances for which existing surface-potential calculation was used. Furthermore, a mixed-mode simulation of an inductive-load demo-circuit was carried out in Silvaco's Mixed-mode for the sake of validation of the proposed model under transient behavior. Comparative analysis of the transient simulations was made by using the model with and without cross-coupling and substrate capacitances. Excellent correlation between model and mixed-mode simulations was observed.

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